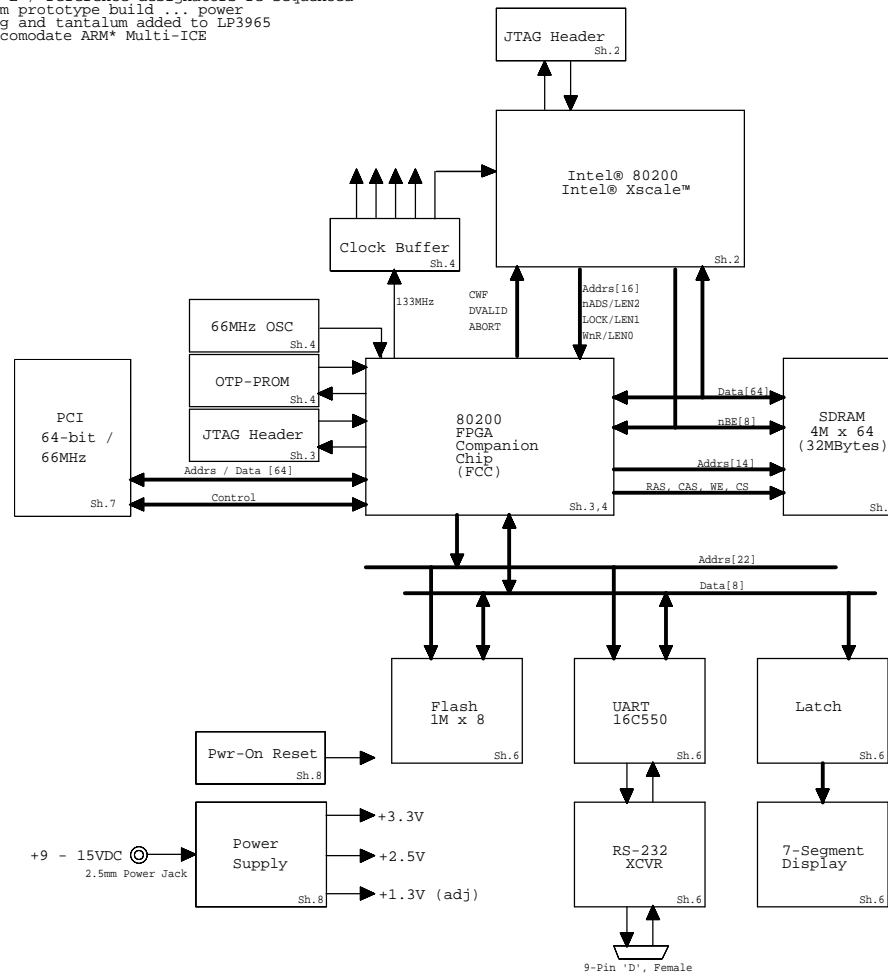


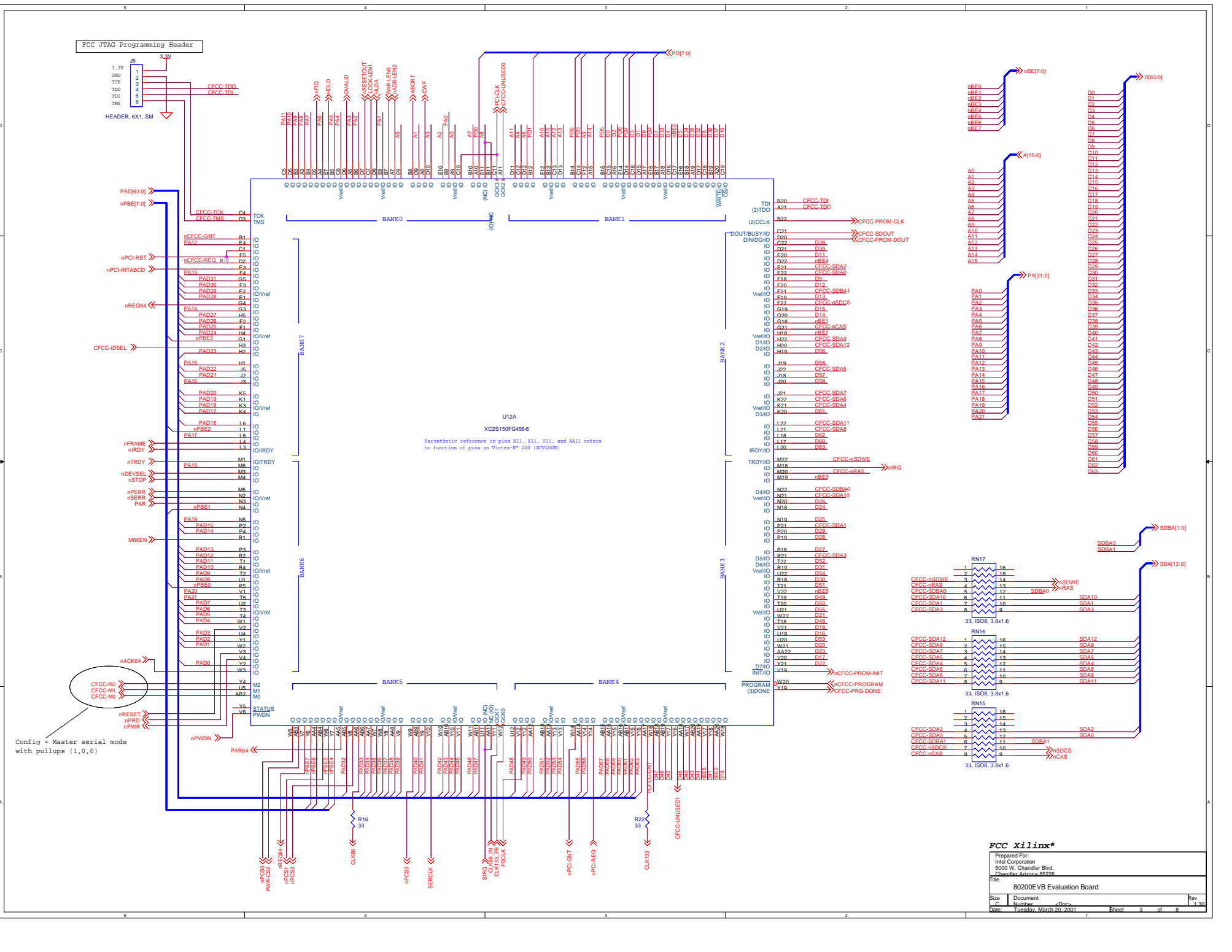
Intel® 80200EVB Revision History

Rev.	Date	Description
0.04	12 Aug 2000	Internal design review
0.05	18 Aug 2000	Review comments incorporated - released for customer review
1.00	25 Aug 2000	Customer review comments incorporated
1.05	22 Sep 2000	Pin and gate swapping - facilitate PCB layout
1.16	29 Sep 2000	Support added for Virtex-E / reference designators re-sequenced
1.20	06 Dec 2000	Changes incorporated from prototype build ... power connector fix. Decoupling and tantalum added to LP3965
1.30	15 Mar 2001	JTAG reset changed to accomodate ARM* Multi-ICE



System Block Diagram

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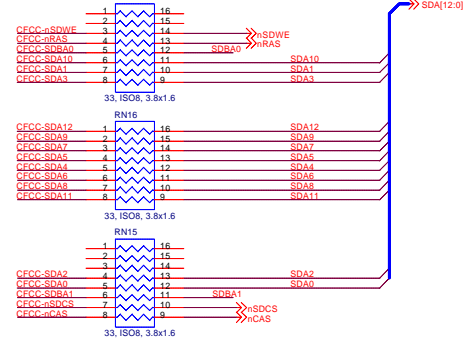
FCC JTAG Programming Header

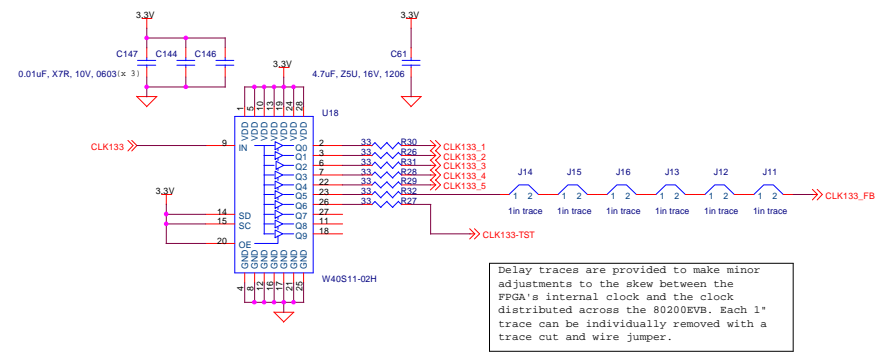
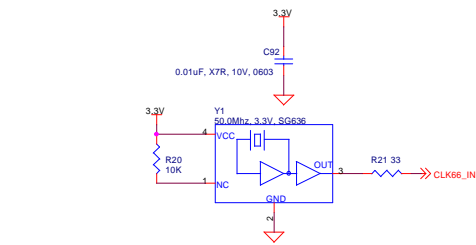
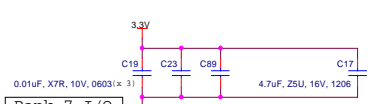
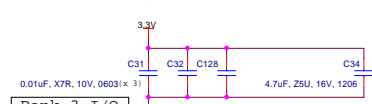
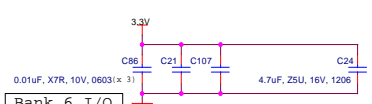
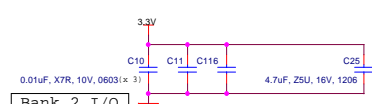
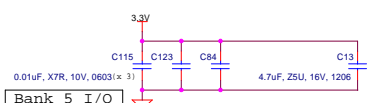
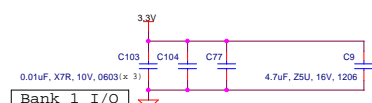
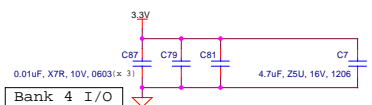
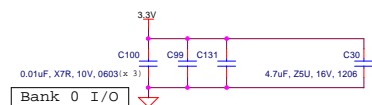
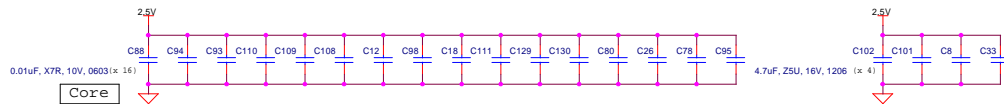
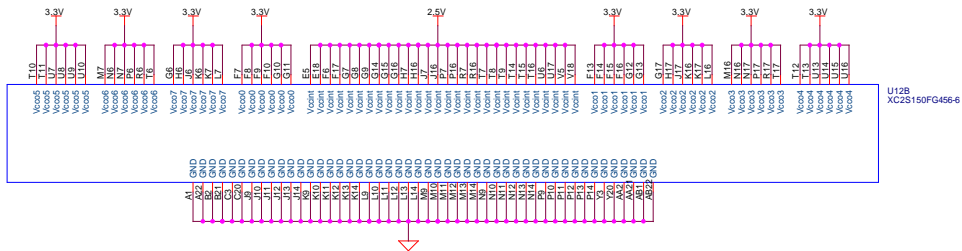


HEADER_6X1_SM

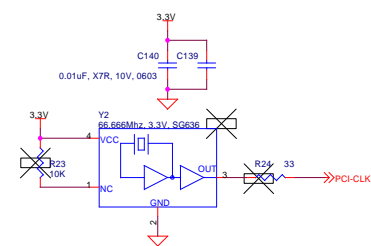
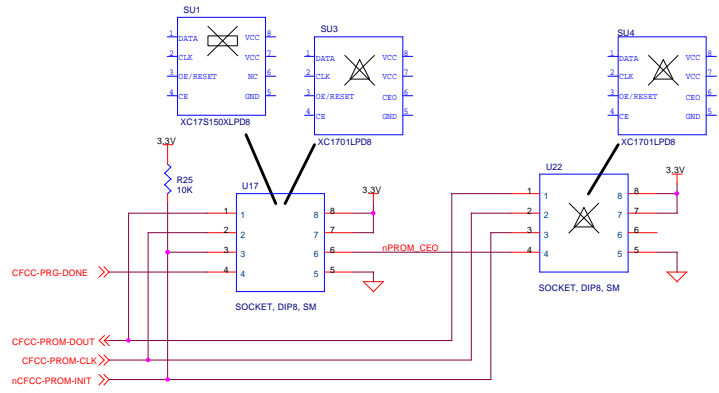
U12A
XC2S150FG456-6
Parenthetic reference on pins B11, E11, U11, and A11 refers to function of pins on Virtex-5 200 (XCV2000E)

Config = Master serial mode with pullups (1,0,0)





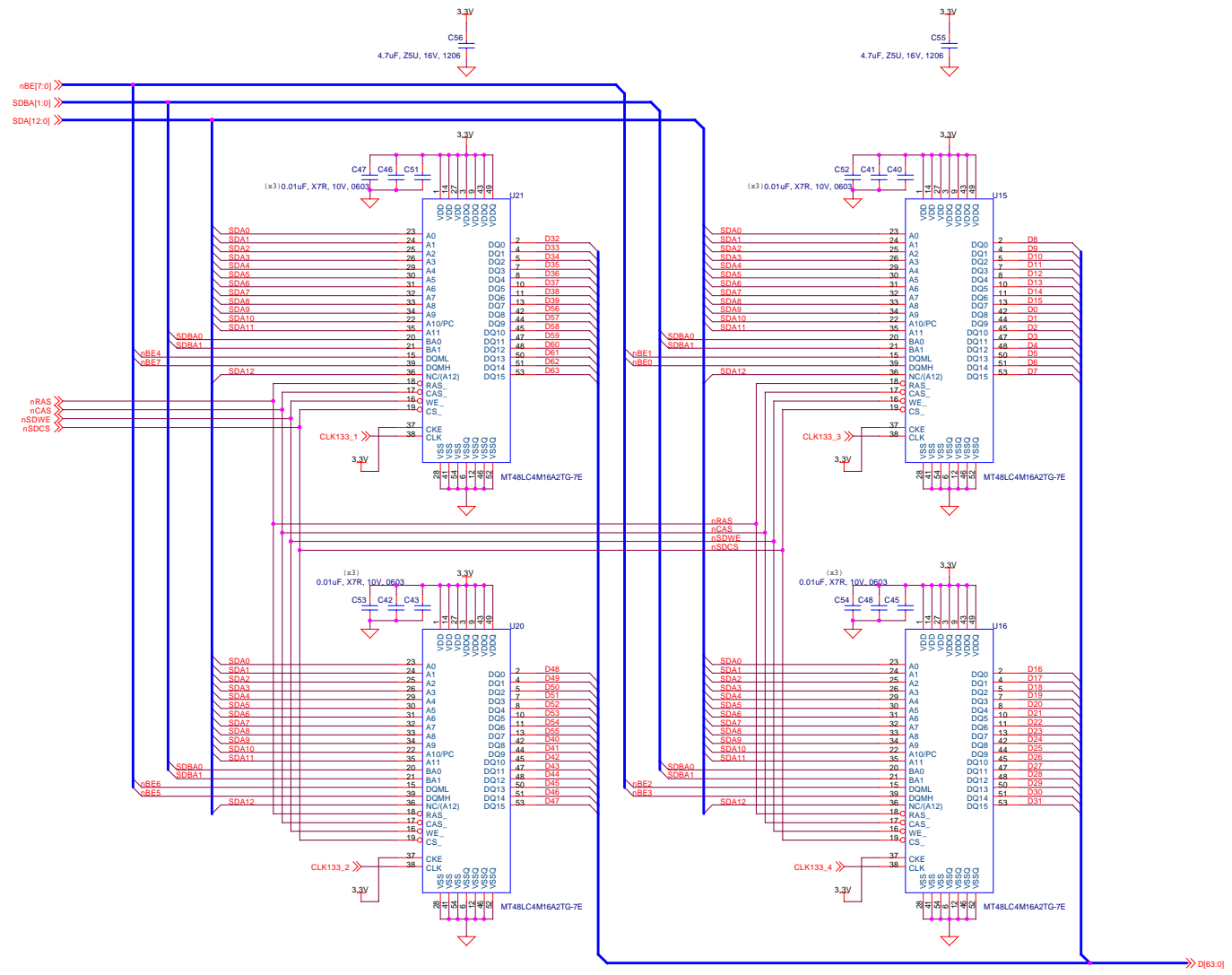
Delay traces are provided to make minor adjustments to the skew between the FPGA's internal clock and the clock distributed across the 80200EVB. Each 1" trace can be individually removed with a trace cut and wire jumper.




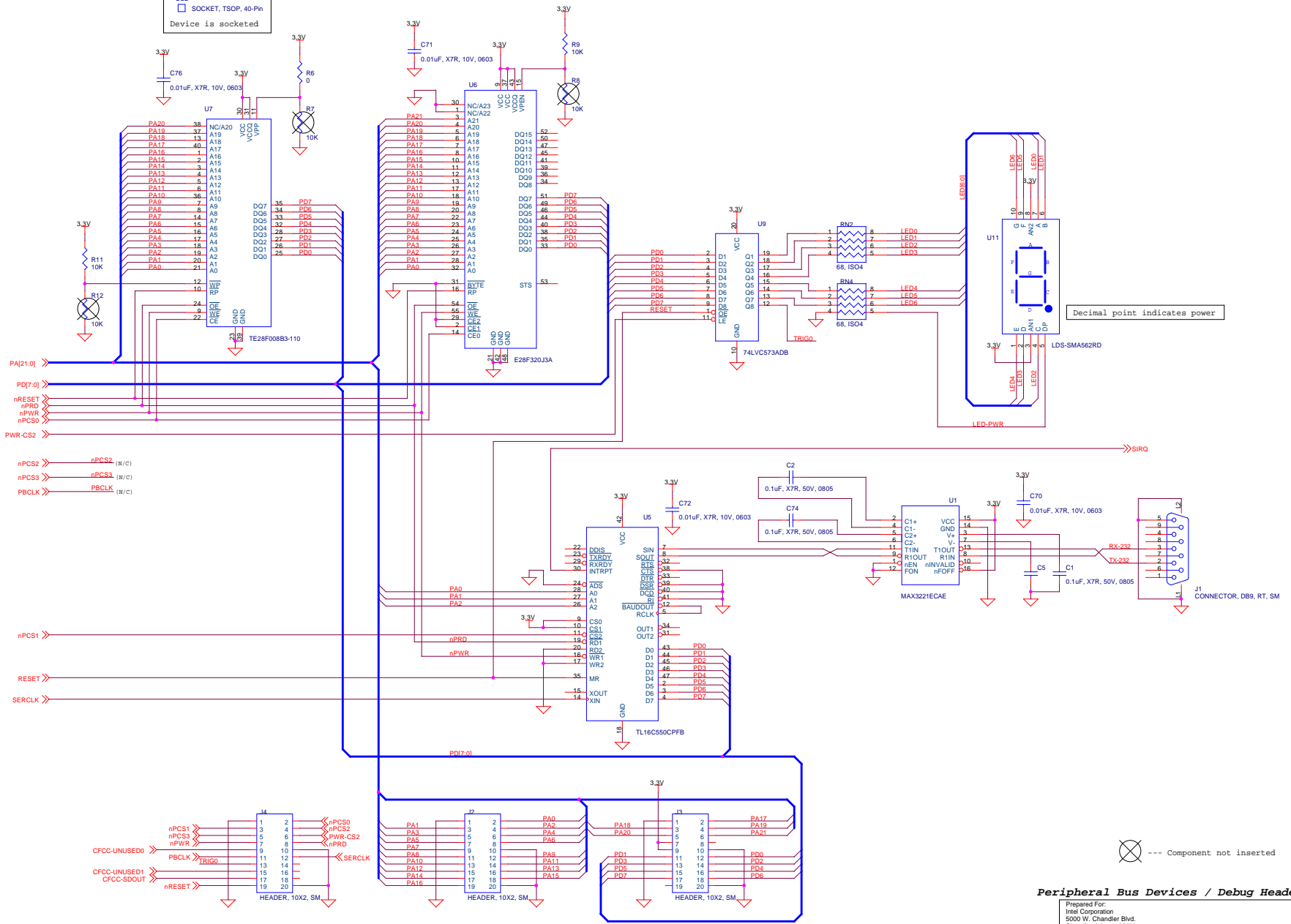
⊠ --- Component not inserted, Virtex-E* version
 ⊠ --- Component not inserted, Spartan-2* version

FCC Power / Clock Generation

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SU2
 SOCKET, TSOP, 40-Pin
 Device is socketed



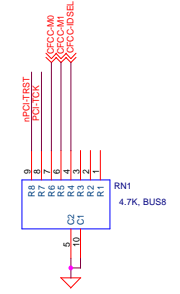
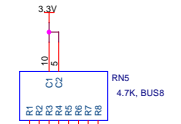
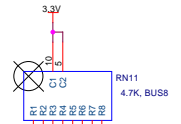
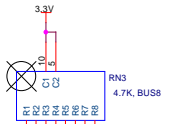
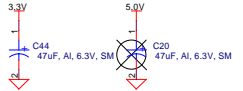
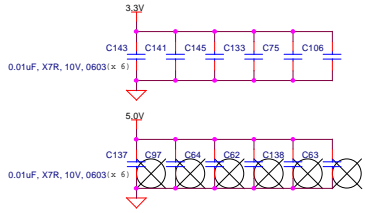
Peripheral Bus Devices / Debug Headers

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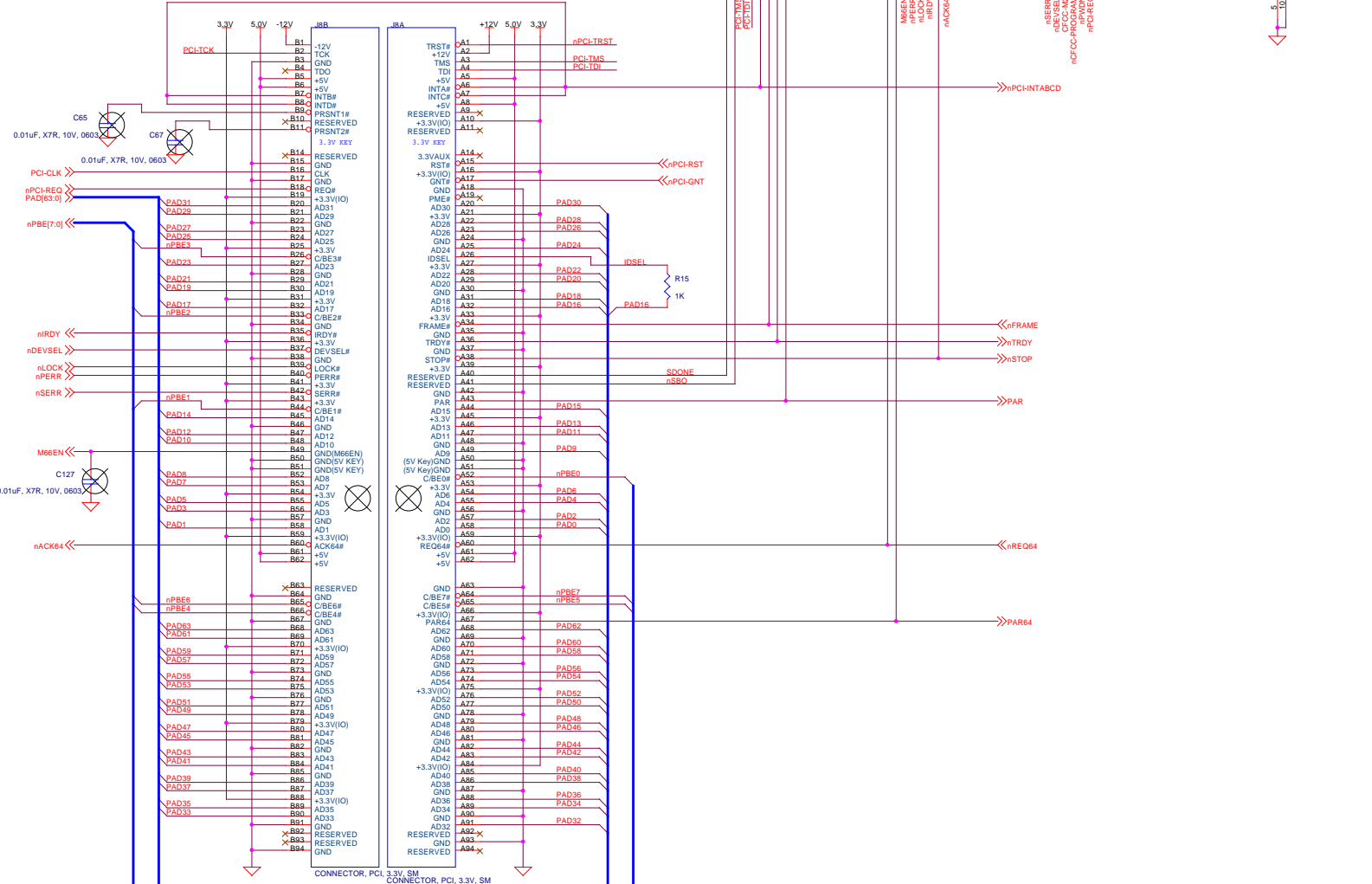
File:
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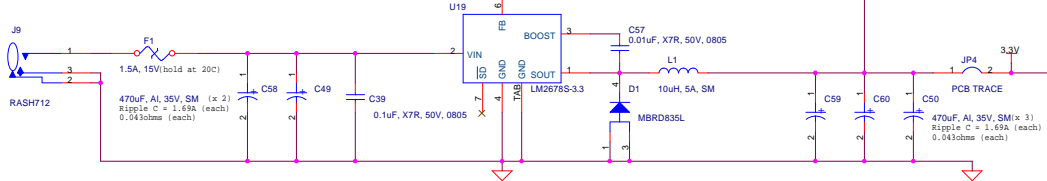
PCI64 CONNECTOR



⊗ --- Component not inserted

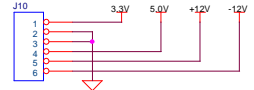
PCI Connector			
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9-to-15VDC
+ = Center pin

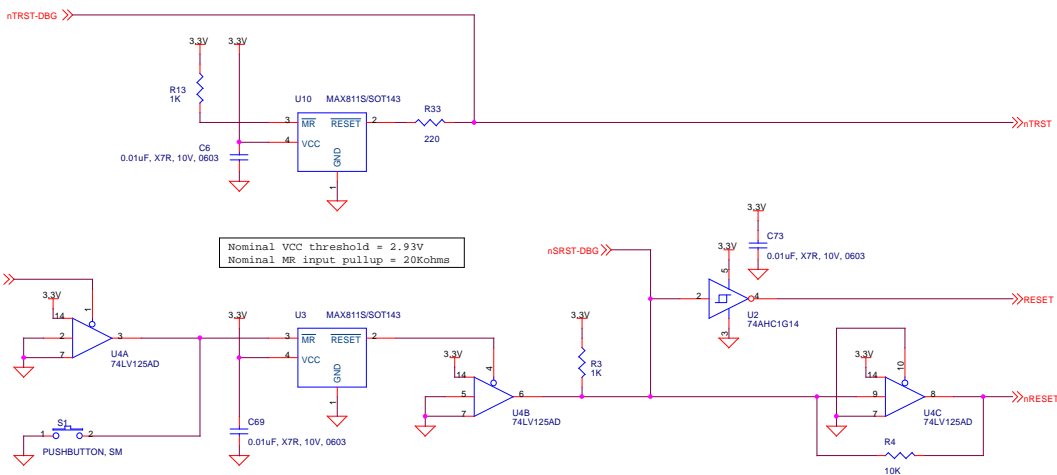
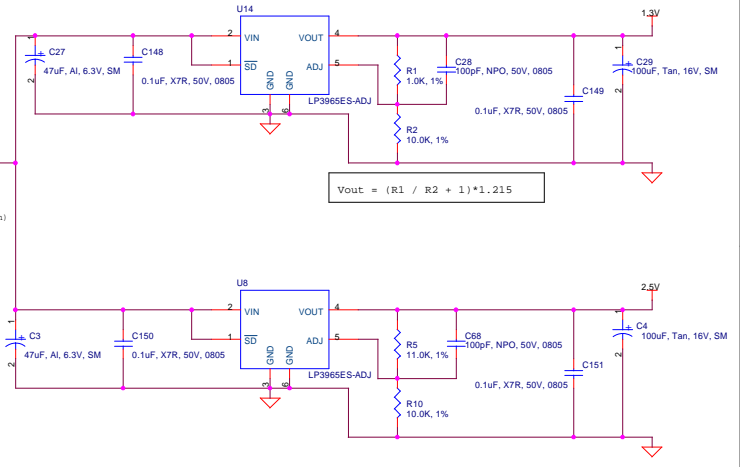


$$V_{out} = (R1 / R2 + 1) * 1.215$$

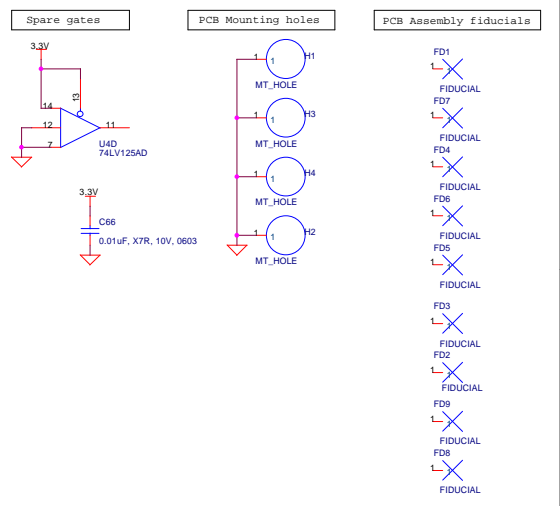
External Power Supply Connector.
Cut JP4 prior to using external 3.3V supply.



CONNECTOR, SCREW TERM, 6 POS



Nominal VCC threshold = 2.93V
Nominal MR input pullup = 20Kohms



Power Supply / Reset	
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