



Intel® IOP315 I/O Processor Chipset with Intel® XScale™ Technology

Dramatically Increases Performance

Product Highlights

Intel® 80200 processor

- 32-bit high-performance CPU (200, 400, 600, 733 MHz)
- ARM* v.5TE compliant
- Intel® Superpipelined RISC Technology – high core speeds with low power
- 32 KB data and instruction caches
- 2 KB Mini data cache for accelerated streaming
- Extended temperature (-40 to +85 degrees)

Intel® 80314 companion chip

- Intel® XScale™ core support (one or two 80200 processors)
- ECC-protected, dual-ported 200 MHz memory controller with support for 3 DIMMs (up to 12 GB), 4 physical (8 logical) banks, 32-page interleaving
- (2) 64-bit-capable PCI/PCI-X interfaces with bridging, arbitration and cPCI hot-swap support
- Switch fabric network (SFN) architecture allowing concurrent DMA, CPU, PCI-X, Gigabit Ethernet and Local Bus accesses
- (2) Gigabit Ethernet MACs, half-/full-duplex support at 10/100 Mb and full-duplex 1 Gb; GMII management interface
- 1 MB low-latency parity-protected on-chip SRAM with direct core or SFN access
- Central 4-channel DMA engine with iSCSI CRC32C and RAID5 XOR (up to 16 sources) off-load engines
- Flexible endian support
- 32-bit, up to 133 MHz Peripheral Bus Interface (PBI) with 4-chip selects
- 1025 HSBGA (40 mm x 40 mm)

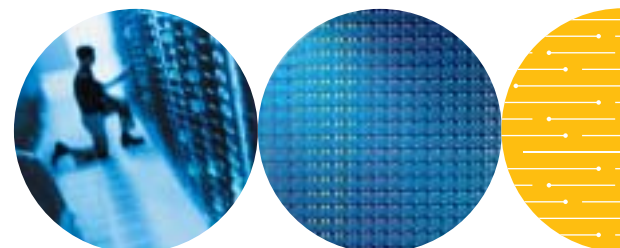


New Intel® 80314 companion chip unleashes Intel® XScale™ technology performance

The Intel® IOP315 chipset — Intel® 80200 processor and Intel® 80314 companion chip — dramatically improves upon the performance of the first-generation I/O processor chipset (Intel® IOP310).

The IOP315 2-chip combo touts a 60 percent performance increase over the previous pair. The performance is scalable with either single or dual core options. Thanks to the Intel XScale microarchitecture, developers of a variety of applications can optimize the needs from ultra-low power of high-performance processing. This new microarchitecture is compliant with the ARM* Version 5TE instruction set (excludes the floating-point instruction set).

Intel in
Communications



High-performance companion chip for the Intel® 80200 processor

The Intel 80314 companion chip for the Intel 80200 processor provides a rich peripheral set designed for storage and network applications. The Intel 80314 can support either one or two Intel 80200 processors. The Intel 80314 uses an internal switch fabric and supports concurrent transactions from any interface to any other interface. For fast memory transactions, the Intel 80200 processor interface has a dedicated bus to the DDR SDRAM memory controller that allows multiple concurrent outstanding transactions.

The Intel 80314 is especially well suited for high-performance storage applications such as network storage target devices (SAN, iSCSI, NAS) and intelligent network adapter cards (iSCSI, IPv4, IPv6, IPSec). The integrated PCI-X bridge, dual-ported ECC memory, low-latency 1 MB SRAM, high-bandwidth switch fabric and CRC32C and XOR engines make it an ideal choice for these applications. In addition, the Intel 80314 is an excellent solution for embedded and networking applications with its integrated dual-10/100/1000 Mbps MACs and flexible endian support.

The Intel® 80200 processor – greater I/O performance through faster cores

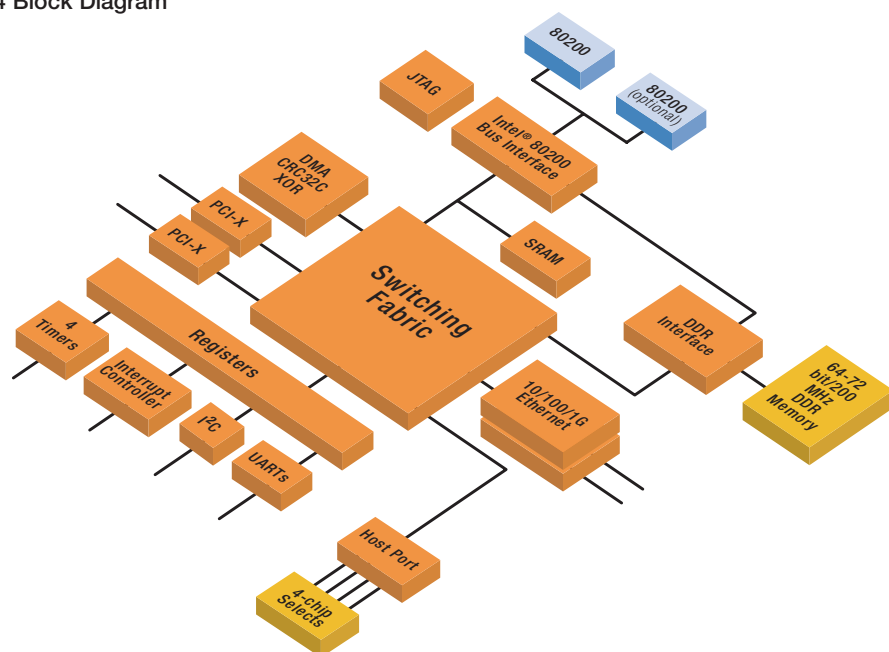
The Intel 80200 processor based on Intel XScale microarchitecture has four speed grades: 200 MHz, 400 MHz, 600 MHz and 733 MHz. This will allow developers to balance performance with power. Even at 600 MHz the 80200 processor dissipates less than a watt! This is accomplished using the Intel Superpipelined RISC Technology – the 7-stage integer, 8-stage memory superpipelined core achieves high speed and ultra-low power.

Not only does this processor have great core speeds, but also 32 KB data and instruction caches. A 2 KB mini-data cache is also included to help avoid “thrashing” of the data cache for frequently changing data streams. The combination of speed and larger caches allows users to implement complex applications and processor-intensive calculations like audio encode/decode or video compression/ decompression.

The 80200 processor based on Intel XScale microarchitecture is code compatible with the SA110. It is also compliant with ARM® v.5TE ISA, so users can maximize code density. The “T” in v.5TE, stands for Thumb® instruction set. The ARM® v.5TE ISA executes either a 32-bit ARM instruction set or a 16-bit Thumb instruction set.

The 80200 processor is tailored for Intel’s world-class manufacturing processes.

Intel® 80314 Block Diagram



Intel® I/O Processor Comparison

	Intel® IOP315 I/O Processor Chipset	Intel® IOP310 I/O Processor Chipset	Intel® IOP321 I/O Processor	Intel® IOP331 I/O Processor
Intel® XScale™ Core	External – can support one or two Intel® 80200s	External – can support one Intel 80200	Integrated	Integrated
Core Speed	400 MHz, 600 MHz, 733 MHz	400 MHz, 600 MHz, 733 MHz	500 MHz, 667 MHz, 800 MHz	500 MHz, 667 MHz, 800 MHz
Chip Count	2-Chip Solution (Intel 80200 & Intel® 80314)	2-Chip Solution (Intel 80200 & Intel® 80312)	1-Chip Solution (w/o Bridge)	1-Chip Solution (w/ Bridge)
Package Size	40 mm x 40 mm and 23 mm x 23 mm	42.5 mm x 42.5 mm and 23 mm x 23 mm	35 mm x 35 mm	37.5 mm x 37.5 mm
Integrated Bridge	133 MHz, 64-bit PCI-X Bridge	66 MHz, 64-bit PCI - PCI Bridge	133 MHz, 64-bit PCI-X Interface	133 MHz, 64-bit PCI-X Bridge
Memory Controller	Dual-ported 200 MHz DDR	100 MHz SDRAM	200 MHz (1.6 GB/s) Bus	Dual-ported DDR 333 MHz/ DDRII 400 MHz
Max Memory	12 GB	512 MB	1 GB	2 GB (DDR); 1 GB (DDR II)
Internal Bus Frequency	133 MHz Switching Fabric	100 MHz (800 MB/s) Bus	200 MHz Bus	266 MHz (2.1 GB/s) Bus
Integrated Memory	1 MB low-latency SRAM	None	None	None
Local Bus Width	32 Bits (up to 133 MHz)	8 Bits (asynchronous bus)	32 Bits (up to 100 MHz)	8/16 Bits (up to 66 MHz)
DMA Buffer Size	4 x 256 Bytes	256 Bytes	1024 Bytes	1024 Bytes
ATU Buffer Size	4 x 1024 Bytes	512 Bytes	4096 Bytes	4096 Bytes
Application Accelerator w/ XOR capability	Yes	Yes	Yes	Yes
PC Bus Interface Unit	2 Serial Units	1 Serial Unit	2 Serial Units	2 Serial Units
Hardware-based CRC32C off-load	Yes	No	No	Yes
Integrated Ethernet MAC	(2) 10/100/1000 Mbps	None	None	None
Timers	4 – 32-bit	None	2 – 32-bit	2 – 32-bit
UART	2 – 9-Pin (16550)	No	SPI	2 – 4-Pin (16550)
GPIO	8 Pins	8 Pins	8 Pins	8 Pins
External Interrupt Pins	16	4	5	17

Intel® 80314 Product Overview

The Intel 80314 introduces a powerful combination of technical advancements. The 64-bit true switch fabric network (SFN) allows multiple concurrent transactions. The SFN offers scalable frequency, 4-deep transaction queues (256B or 1kB) with burst sizes up to 1kB supported. Store and forward to the SFN and immediate drain from the SFN are supported. The integrated bridge (PCI/PCI-X) can configure devices on either bus, with each side capable of operating at different frequencies, 33 MHz to 133 MHz, and in either mode, PCI or PCI-X. The 80314 has 4 address spaces with translation managed via highly configurable sets of registers. It contains a 32-bit peripheral bus interface (PBI) (programmable up to 133 MHz) that is great for embedded applications requiring a connection to non-PCI peripheral components such as ASICs, flash memory, PLDs, or DSPs.

The dual-ported SDRAM memory controller unit (MCU) is vastly improved over previous IOP generations with core-to-memory performance greater than 5 times faster! The interface runs at 200 MHz. It offers two-port (64-bit data, 36-bit address) concurrent access to memory with programmable arbitration for each port. It has support for up to 4 physical (8 logical) banks and has up to 32-page interleaving. The MCU has optional ECC and supports up to 12 GB (3 DIMMs) DDR SDRAM.

The 80314 integrates a 4-channel DMA controller with support for unaligned transfers using both scatter-gather and direct modes. Data can be transferred to or from any SFN port. The DMA engines also support offloading of RAID5 XOR and iSCSI CRC32C operations.

The 80314 features (2) 10/100/1000 Mbps Ethernet MACs that fully support standards IEEE 802.3, 802.3u, 802.3x, 802.3z, and 802.3ac. Both full- and half-duplex modes are supported at 10/100 Mbps. Full duplex is supported at 1 Gbps.

The 80314 features an option of integrated 1 MB very low- latency SRAM that has either direct core or SFN access. The SRAM BAR has priority for 80200 Bus Interface unit address claiming. The SRAM is application-independent, so it can be used for a variety of applications.

The 80314 also integrates a Multi-Processor Interrupt Controller (MPIC) with 24 interrupt inputs (16 external, 8 internal), 4 dedicated outputs, 16 priorities, 4 global 32-bit timers, 4 doorbell registers, and 4 general-purpose mailbox registers. Additional interfaces include I²C, 2 UART ports, and a JTAG interface. This integration helps reduce chip count, saves board space and simplifies designs.

Please reference the most up-to-date Order Configurations and Regulatory Compliance Specifications along with additional product information at developer.intel.com/design/storage

Features

Benefits

<p>Intel® 80200 Interface</p> <ul style="list-style-type: none"> ■ 100 MHz Request Bus ■ 4-Entry Request Buffer ■ 2.5V I/O generation, 3.3V tolerant (from Intel 80200) ■ Support for single or dual Intel 80200 processors ■ ECC-based bus integrity protection 	<p>High-performance Intel® XScale™ technology that scales</p>
<p>Dual PCI/PCI-X Interfaces</p> <ul style="list-style-type: none"> ■ Integrated PCI-X bridge ■ 25-133 MHz operation ■ 4 DMA units with chaining support ■ Support to configure the device from remote PCI host ■ CPCL hot-swap support ■ 5V tolerant/3.3V I/O ■ 4 concurrent split transactions ■ Configurable arbitration logic 	<p>PCI-X to PCI-X bridge integration lowers Bill of Material (BOM) cost and helps reduce board space</p> <p>Provides for increased system concurrency</p>
<p>Optimized Memory Controller</p> <ul style="list-style-type: none"> ■ Dual-ported MCU ■ 64- and 72-bit memory ■ 12 GB support, 3 DIMMs 	<p>Dramatically increases core to memory performance</p>
<p>Optional 1 MB of Low-Latency SRAM</p>	<p>Low-latency memory option helps reduce bottlenecks and improve performance</p>
<p>Communications</p> <ul style="list-style-type: none"> ■ 2 GbE MACs ■ 133 MHz, 32-bit local bus with 4-chip selects ■ I²C ■ UARTs ■ 8 GPIO pins 	<p>Integration reduces board space, lowers BOM, and improves performance</p>
<p>Application Accelerator Units in DMA</p> <ul style="list-style-type: none"> ■ RAID5 XOR ■ iSCSI CRC32C 	<p>Storage-specific integration in hardware improves performance and helps reduce CPU overhead</p>

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