



Intel[®] 80315 I/O Processor

Design Checklist

January 2005





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Revision History

Date	Revision	Description
January 2005	001	Initial release

Introduction

1

This checklist is a compilation of key signals and strap options. It is not meant to be a complete signal list or a substitute for proper study of available design guides, documentation, or reference schematics. The high speed clocking required when designing with the 80314 requires special attention to signal integrity. In fact it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. Designers should use this guide in conjunction with *Intel® GW80314 I/O Companion Chip Design Guide* and the *Intel® IQ80315 Evaluation Platform Board Schematics*.

1.1 List of References

Table 1. List of References

Document	Document Number
Intel® 80314 Datasheet	http://developer.intel.com/design/iio/datashts/273757.htm
Intel® 80314 Developer's Manual	http://developer.intel.com/design/iio/manuals/273756.htm
Intel® 80314 Specification Update	http://developer.intel.com/design/iio/specupdt/273759.htm
Intel® IQ80315 Evaluation Platform Board Schematics	http://developer.intel.com/design/iio/schems/IQ80315Schem.htm
Intel® 80200 Processor based on Intel XScale® Microarchitecture Developer's Manual	http://developer.intel.com/design/iio/manuals/273411.htm
Intel® 80200 Processor based on Intel XScale® Microarchitecture Datasheet	http://developer.intel.com/design/iio/datashts/273414.htm
Intel® 80200 Processor based on Intel XScale® Microarchitecture Specification Update	http://developer.intel.com/design/iio/specupdt/273415.htm
Intel® GW80314 I/O Companion Chip Design Guide	http://developer.intel.com/design/iio/designex/273758.htm
PCI Local Bus Specification, Revision 2.3	http://www.pcisig.com/specifications/conventional_pci
PCI-X revision 1.0a	http://www.pcisig.com/specifications/pci_x
PCI-X Compliance Checklist	http://www.pcisig.com/data/specifications/pci_x_checklist_1_0_a.doc
PCI 2.2 Compliance Checklist	http://www.pcisig.com/data/specifications/2_2_checklist.doc

Intel® 80314 Companion Chip and 80200 Intel XScale® Processor Checklist 2

This section provides checklist information.

Table 2. 80200 Intel XScale® Processor Checklist

Category	Guideline	Compliance	
		Yes	No
CLK	Intel® 80200 processor core input clock must be 66 MHz. When required, it could go down to 50 MHz. When < 50 MHz, the 3:1 clock ratio is in violation.		
PLLCFG	PLLCFG must be connected to a 4.7 K pull-up.		
CWF	CWF must be connected to a 4.7 K pull-down or to a 80314 XS_CWF pin.		
HOLD	For Single Processor Mode HOLD must be connected to a 4.7 K pull-down.		
HOLDA	For Single Processor HOLDA is NC		
LOWVPP	LOWVPP must be connected to a 4.7K Pull-down		
LOWVCC	LOWVCC must be connected to a 4.7K Pull-down		
MCLK (Single Processor)	The trace connection from the 80314 XS_CLK pin to the 80200 MCLK pin should be length matched to the longest Data or Address line. Series termination of 10 OHMS should be placed as close as possible to the 80314. Parallel termination of 60 OHMS should be placed close to the 80200. Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more details.		
MCLK (Dual Processor)	The trace connection from the 80314 XS_CLK pin to the 80200 MCLK pin should be length matched to the longest Data or Address line. Series termination of 60 OHMS should be placed as close as possible to the 80314. There is no Parallel termination when using Dual Processors. Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more details.		
IRQ# and FIQ#	IRQ# and FIQ# must be connected to 4.7 K pull-up.		
VCCA	VCCA must have a filter. Refer to the <i>Intel® 80200 Processor Intel XScale® Microarchitecture Datasheet</i> for more details.		
VCCP	Power sequencing must be followed. VCCP must be brought up the same or before VCC . Refer to the <i>Intel® 80200 Processor Intel XScale® Microarchitecture Datasheet</i> for more details.		

Table 3. 80314 Companion Chip Checklist (Sheet 1 of 6)

Category	Guideline	Compliance	
		Yes	No
PCI BUS			
IDSEL	If the source bridge requires IDSEL inputs to be resistively coupled to AD bits, those resistors have a value of 2K ohms or less. Devices 1-4 connect to AD[17] through AD[20] respectively, AD[16] is typically reserved for the PCI/PCI-X bridge.		
PCIXCAP	<p>Platform level logic must translate the PCIXCAP level into the 2 bit Px_PCIXCAP[1:0] signals which latch on the rising edge of P_RST#. Circuitry for this translation will vary. Fully embedded designs (no slots) may simply strap Px_PCIXCAP[1:0] to the desired PCI/X mode. Designs with variable configurations such as slots, will need to translate/decode PCIXCAP voltage ranges to Px_PCIXCAP[1:0] logic levels. Refer to the <i>Intel® IQ80315 I/O Processor Evaluation Platform Schematics</i> for more details.</p> <p>When Px_RSTDIR = 0, the PCI/X block detects when its PCI interface is configured as a PCI-X agent by latching the PCI-X initialization pattern as defined by PCI-X 1.0a Addendum. The port latches the initialization pattern on the rising edge of P_RST#.</p> <p>When Px_RSTDIR = 1, the PCI/X block drives its PCI interface to indicate configuration as a PCIX or PCI 2.3 bus. The PCI/X block drives the initialization pattern on the rising edge of P_RST# based on the state of PCI/X CAP[1:0].</p> <p>Refer to the <i>Intel® 80314 I/O Companion Chip Developer's Manual</i> for more details.</p>		
Px_PCIXCAP[1:0]	If a system includes slots for add-in cards, the system must provide a circuit for sensing the connection of the PCIXCAP pin of all add-in cards. Refer to the <i>Intel® IQ80315 I/O Processor Evaluation Platform Schematics</i> for more details.		
P_M66EN	<p>P_M66EN is used to indicate the operating frequency of the PCI 2.3 interface. P_M66EN is sampled on the rising edge of P_RST#.</p> <p>P_M66EN = 0 – 33MHz P_M66EN = 1 – 66MHz</p>		
PCI-X Bus Frequencies	<p>Design considerations for PCI-X bus frequencies. Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more details.</p> <p>133 Mhz – 2 Maximum loads 100 Mhz – 4 Maximum loads 66 Mhz -- 8 Maximum loads.</p>		
Px_LOCK#	8.2 K Pull-up P2_LOCK is not an 80314 signal but it should have a pull-up if it is on the board and the application is not a PCI adapter card.		
Px_Reqx#	8.2 K Pull-up		
Px_INTx#	8.2 K Pull-up		
Px_SERR#	8.2 K Pull-up ^a		

Table 3. 80314 Companion Chip Checklist (Sheet 2 of 6)

Category	Guideline	Compliance	
		Yes	No
Px_TRDY#	8.2 K Pull-up ^a		
Px_PERR#	8.2 K Pull-up ^a		
Px_DEVSEL#	8.2 K Pull-up ^a		
Px_FRAME#	8.2 K Pull-up ^a		
Px_STOP#	8.2 K Pull-up ^a		
Px_IRDY#	8.2 K Pull-up ^a		
Px_INT[A:D]#	8.2 K Pull-up ^a		
Px_AD[63:32]	8.2 K Pull-up ^a		
Px_C/BE[7:4]#	8.2 K Pull-up ^a		
Px_PAR64	8.2 K Pull-up ^a		
Px_REQ64#	8.2 K Pull-up ^a		
Px_ACK64#	8.2 K Pull-up ^a		
Px_M66EN	8.2 K Pull-up ^a		
Memory Interface			
SD_CKFBO SD_CKFBI	The receive enable out pin SD_CKFBO must be connected to the receive enable in pin SD_CKFBI. The SD_CKFBI trace length should be three inches		
Source Synchronous SD_DQ[63:0], DM[8:0] SD_DQS[8:0], CB[7:0]	Rs = 10 Ohm +/- 5% Rp = 56 Ohm +/-1% The 80314 source synchronous signals are divided into groups consisting of data bits SD_DQ and check bits SD_CB. There is an associated strobe SD_DQS for each SD_DQ, DM and SD_ECC group. When data masking is not used, system memory SD_DM pins on the DDR should be tied to ground. Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more details on grouping.		
Common Clocked SD_CLK[2:0] SD_CLK[2:0]#	Rs = 22 ohms +/- 5% ohms Rp = 120 ohms +/- 1% (Rp is used for NON-DIMM solutions only). DIMMs have parallel termination on the DIMM		
Source Clocked SD_RAS#, SD_CAS#, SD_WE#, SD_BA[1:0] SD_MA[12:0].	Rs = 22 ohms +/- 5% ohms Rp = 56 ohms +/- 1% Resistor packs are acceptable for the parallel (Rp) control termination resistors but control signals can NOT be placed within the same RPACK as data, strobe, or command signals.		
Chip Selects and Chip Enables CS SD_CKEN#	Rs = 22 ohms +/- 5% ohms Rp = 56 +/- 1%		
Registered DIMM reset	The 80314 does not provide the reset signal required by Registered DIMMs. Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more details on circuits.		

Table 3. 80314 Companion Chip Checklist (Sheet 3 of 6)

Category	Guideline	Compliance	
		Yes	No
Discrete DDR Devices	Use the same guidelines as described for DIMM solutions. However, to compensate for the trace length on the DIMM, add DIMM TLO lengths (which are specified in the PC1600 and PC2100 DDR SDRAM Unbuffered DIMM Design Specification) to the trace lengths specified in the above sections. The same guidelines for routing for each of the control groups can be extrapolated from the above DIMM layout guidelines. Refer to the <i>PC1600 and PC2100 DDR SDRAM Unbuffered DIMM Design Specification</i> for more details on the clock tree. Rs may be combined into a single resistor; tolerance becomes 1%. Rp stub must be connected between Rs and first branch.		
Non-Battery Backup Circuits	For applications that do not support battery back-up, the SD_CLKEN circuit is no longer required. In this case follow these steps: Pull the DDR SD_CLKEN pin high, and leave the SD_CLKEN signals on the 80314 as 'no connects'. This keeps the SDRAM from entering a pseudo, self-refresh mode which can cause a lock-up condition on the SDRAM device.		
Peripheral Bus			
PBI_CS#[3:0]	The PCE0# is the Peripheral Bus chip enable to be used for booting purposes.		
PBI_AD[31:0]	Refer to Table 1 , Table 2 , and Table 3 for PBI_AD pin information.		
Configuration Pull-up/Pull-down			
PWRUP_P1_PRIM	10 K Pull-up, P1 is the primary PCI bus. 10 K Pull-down, P1 is the secondary PCI bus.		
PWRUP_P2_PRIM	10 K Pull-up, P2 is the primary PCI bus. 10 K Pull-down, P2 is the secondary PCI bus.		
PWRUP_XS_SWRST	4.7 K Pull-down -- Controls state of Software Reset inside IntelXScale@microprocessorCIUblock (0 – XScale interface not held in reset). (1 – XScale interface held in reset)		
PWRUP_P1_SWRST	4.7 K Pull-down -- Controls state of Software Reset inside P1 PCI/X block (0 – PCI1 interface not held in reset) (1 – PCI1 interface held in reset until cleared by processor)		
PWRUP_P2_SWRST	4.7 K Pull-down -- Controls state of Software Reset inside P2 PCI/X block (0 – PC21 interface not held in reset) (1 – PCI2 interface held in reset until cleared by processor)		
PWRUP_P1_ARB	4.7 K Pull-up -- Enable PCI 1 arbiter (0 - Arbiter not enabled) (1 - Arbiter enabled)		

Table 3. 80314 Companion Chip Checklist (Sheet 4 of 6)

Category	Guideline	Compliance	
		Yes	No
PWRUP_P2_ARB	10 K Pull-up -- Enable PCI 2 arbiter (0 - Arbiter not enabled) (1 - Arbiter enabled)		
PWRUP_PBI_BSWP	4.7 K Pull-down -- Disable Intel XScale® byte swap mode		
PWRUP_TRANS	4.7 K Pull-down -- Embedded Mode Operation (Transparent mode is not supported)		
P1_RSTDIR	4.7 K Pull-up Reset Direction: 0 = P1_RST# is input and P1_CLK_OUT is driven to 0. 1 = P1_RST# is output and P1_CLK_OUT is generated (PCI Port 1 is controlling resource).		
P2_RSTDIR	10 K Pull-up Reset Direction: 0 = P2_RST# is input and P2_CLK_OUT is driven to 0. 1 = P2_RST# is output and P2_CLK_OUT is generated (PCI Port 2 is controlling resource).		
XS_HOLD[1:0]	4.7 K Pull-down		
XS_HLDA[1:0]	For single processor configuration, XS_HLDA[0] should be tied low and XS_HLDA[1] should be tied high. Connect directly to 80200 processors for dual configuration.		
XS_FIQ0	4.7 K Pull-up		
XS_FIQ1/ PWRUP_SD_BYP	4.7 K Pull-down - Interrupt: indicates a fast interrupt to processor 1. During powerup this pin is latched at the rising edge of reset and used to enable the SDRAM PLL bypass mode when latched high.		
IRQ[1]/ PWRUP_XS_BYP	4.7 K Pull-down - Interrupt: indicates a interrupt to processor 1. During powerup this pin is latched at the rising edge of reset and is used to enable the Intel XScale® microprocessor PLL bypass mode when latched high.		
IRQ[0]/ PWRUP_FADJ	During powerup this pin is used to program Intel XScale® microprocessor PLL frequency adjust logic. PWRUP_FADJ = 0, Intel XScale® PLL Frequency = 3/4 * FN_CLK PWRUP_FADJ = 1, Intel XScale® PLL Frequency = SFN_CLK.		
TRST#	1.5K pull-down* Alternatively tied to P_RST#. Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more information on using an ICE. When not used, this signal should be tied to GND.		
SD_I2C_SDA	This signal is internally Pulled High.		
SD_I2C_CLK	This signal is internally Pulled High.		
I2C_SCLK	This signal is internally Pulled High.		

Table 3. 80314 Companion Chip Checklist (Sheet 5 of 6)

Category	Guideline	Compliance	
I2C_SDA	This signal is internally Pulled High.		
Hot Plug Signals			
		Yes	No
Px_ENUM#	8.2 K Pull-up System Enumeration: Used to notify system host that a board has been freshly inserted or extracted from the system.		
Px_ES	8.2 K Pull-down Ejector Switch: Indicates the status of Hot Swap board ejector switch.		
Px_HEALTHY#	1 K Pull-down Board healthy - In a CPCI Hot Swap environment, indicates the board is ready to be released from reset and become an active agent on the PCI bus. Negation of P1_HEALTHY# resets all GW80314 resources, including PLLs. Additionally, all GW80314 outputs are tristated when this pin is negated; some inputs and bi-directionals are inhibited.		
Px_HS_64EN#	8.2 K Pull-up PCI/X 64-bit Enable: An active low indication that a CompactPCI Hot Swap board is in a 64-bit slot.		
Px_LED#	8.2 K Pull-up LED: Controls the Hot Swap status LED.		
Gigabit Ethernet Interface			
Ex_TCG[9:0]	Rs (Series Resistor) should be 33 Ohms (+/- 5%)		

Table 3. 80314 Companion Chip Checklist (Sheet 6 of 6)

Category	Guideline	Compliance	
Unused Ports	Unused inputs get tied low for unused GigE. (e.g. GigE 0: E0_RCG[x:x], E0_RCG, E0_PCRS_SDET, E0_PRBS_PASS, E0_RXCLK.)		
Power Delivery			
	<p>There are nine different voltage domains needed. XS_PLL_AVCC, SD_PLLAVCC, P1_PLLAVCC and P2_PLL_AVCC are similar in that they <i>each</i> require a separate VCC33 supply for the phase lock loop of the Intel XScale® clock, DDR clock, PC11 clock, and PC12 clock generators, respectfully. To reduce noise-induced clock jitter, add a simple bypass filter circuit, to each line.</p> <p>VREF SDRAM voltage reference is used to supply the reference voltage to the differential inputs of the memory controller. This voltage is generated by a resistor divider circuit off the 2.5 V.</p> <p>VCC33 3.3V Power connects to a 3.3V powerboard plane, VCC25 2.5V Power connects to a 2.5V powerboard plane and VCC_CORE 1.5V Power connects to a 1.5 V powerplane.</p> <p>VTT DDR Termination Resistor voltage is 1.25 V.</p> <p>Refer to the <i>Intel® 80314 I/O Companion Chip Design Guide</i> for more information.</p>		

a. An add-in card may rely on the motherboard to pull-up these signals on the HBA side.

Table 1. PBI_AD 8-bit Mode

PBI_AD Pins	31 24	23 16	15 8	7 4	3 0
Address Phase	A27 - A20	A19 - A12	A11 - A4	A3 - A0	A23 - A20
Data Phase	D7 - D0	A19 - A12	A11 - A4	A3 - A0	A23 - A20

Table 2. PBI_AD 16-bit Mode

PBI_AD Pins	31 24	23 16	15 8	7 5	4	3	2	1 0
Address Phase	A27 - A20	A19 - A12	A11 - A4	A3 - A1	x	x	x	B1 B0
Data Phase	D15 - D8	D7 - D0	A11 - A4	A3 - A1	x	x	x	B1 B0

Table 3. PBI_AD 32-bit Mode

PBI_AD Pins	31 24	23 16	15 8	7 6	5	4	3 0
Address Phase	A27 - A20	A19 - A12	A11 - A4	A3 - A1	x	x	B3 B0
Data Phase	D32 - D24	D23 - D16	D15 - D8	D7 - D0			