



Intel[®] 80331/80332 I/O Processors JTAG Support

White Paper

August 2004



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Revision History

Date	Revision	Description
August 2004	002	Added support for 80332.
September 2003	001	Initial release

1.0 Introduction

This document provides information useful for the development of JTAG debug support for the Intel® 80331 and 80332 I/O processors¹ (80331 and 80332) and their respective customer reference boards. It points out key details and specifies where to find more information.

For more information on JTAG and debug for the 80331, refer to Chapter 19, “Test Logic and Testability,” in the *Intel® 80331 I/O Processor Developer’s Manual* (273942).

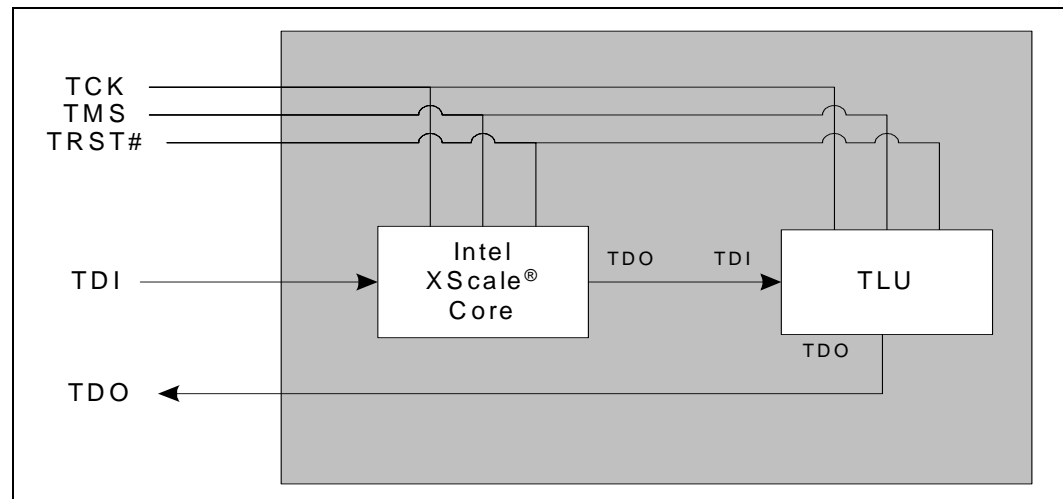
For more information on JTAG and debug for the 80332, refer to Chapter 22, “Test Logic and Testability,” in the *Intel® 80332 I/O Processor Developer’s Manual* (274065).

For information on JTAG and debug relating to the Intel XScale® core, refer to Chapter 13, “Software Debug”, and Appendix C, “Test Features”, in the *Intel® 80200 Processor based on Intel XScale® Microarchitecture Developer’s Manual* (273411).

2.0 Multiple TAP Chain

The 80331 and the 80332 have identical TAP chain configurations. The TAP chain contains two TAP controllers that are connected in a typical daisy-chain configuration. The Intel XScale® core TAP controller is the first TAP in the chain closest to TDI (Figure 1), and the other TAP controller is used for silicon testing and must be placed in bypass.

Figure 1. TAP Controller Configuration



3.0 Evaluation Platform Board TAP Chain

The TAP chains on the 80331 and 80332 customer reference boards have jumper selections that affect them. Refer to the customer reference board manual to set the jumpers and switches properly before connecting with JTAG.

1. ARM* architecture compliant.

4.0 JTAG Connector

The 80331 and the 80332 evaluation platform boards have an ARM-compliant 20-pin connector as illustrated in Figure 2.

Figure 2. 80331 JTAG Connector

VTref	1	2	Vsupply
nTRST	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
RTCK	11	12	GND
TDO	13	14	GND
nSRST	15	16	GND
DBGRQ	17	18	GND
DBGACK	19	20	GND

5.0 JTAG Instructions and Data

The JTAG registers and instruction sets are defined in Section 19.3.4.2, “Instructions,” of the *Intel® 80331 I/O Processor Developer’s Manual* (273942), and in Section 21.3.4.2, “Instructions,” of the *Intel® 80332 I/O Processor Developer’s Manual* (274065). The Intel XScale® TAP controller instructions are 7-bit instructions.

6.0 Flash Programming

Flash programming support for the 80331 and 80332 customer reference boards is required. The customer must be able to select an 80331 or an 80332 configuration file from a directory and program the Flash with a standard format (elf, srec, bin, Intel® hex). The Flash device used on the board is an Intel Strataflash® chip (part number 28F640J3A).

7.0 Register Addresses

Register addresses are needed for Flash programming and for register display by the debugger. The coprocessor registers can be accessed only by “mrc” and “mcr” assembly instructions. Coprocessor instructions are defined in the *Intel® 80200 Processor based on Intel XScale® Microarchitecture Developer’s Manual* (273411). The memory-mapped register addresses are defined in Chapter 17 in the *Intel® 80331 I/O Processor Developer’s Manual* (273942) and in Chapter 17 in the *Intel® 80332 I/O Processor Developer’s Manual* (274065).

8.0 Functionality Standard

The established standard is that the customer should be able to Flash the board with RedBoot* (or some equivalent), run to the RedBoot prompt, load an elf program, and step through that elf application viewing the source code with the debugger.

9.0 Register Display

The debugger must display core, coprocessor, and memory-mapped registers.

10.0 Hot-Debug

Hot-Debug must be functional for the 80331 and the 80332. To support Hot-Debug, the JTAG debugger must have some additional functionality. The details of Hot-Debug are specified in the *Hot-Debug for Intel XScale[®] Core Debug White Paper (273539)* (located at <http://intel.com/design/iio/applnotes/273539.htm>).

11.0 Speeds and Electrical Specifications

The maximum TCK frequency is 25 MHz, and the VTref voltage is 3.3 V. For more information, refer to the *Intel[®] 80331 I/O Processor Datasheet (273943)* and the *Intel[®] 80332 I/O Processor Datasheet (274066)*.

12.0 JTAG IDs

The JTAG IDs for the 80331 are different for each stepping and are found in the identification information section of the *Intel[®] 80331 I/O Processor Specification Update (273930)* located at <http://developer.intel.com/design/iio/docs/iop331.htm>.

The JTAG IDs for the 80332 are different for each stepping and are found in the identification information section of the *Intel[®] 80332 I/O Processor Specification Update (303107)* located at <http://developer.intel.com/design/iio/docs/iop332.htm>.

13.0 Conclusion

For details that are not covered in this document or in the referenced documents, or if you need to order a developer's manual or datasheet, please contact an Intel field sales representative, visit the Intel Contact Support website (<http://support.intel.com/support/9089.htm#northamerica>), or call (916) 377-7000.

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