

Intel(R) IQ80332 I/O Processor DDR-II 400 Evaluation Platform Board (IQ80332)

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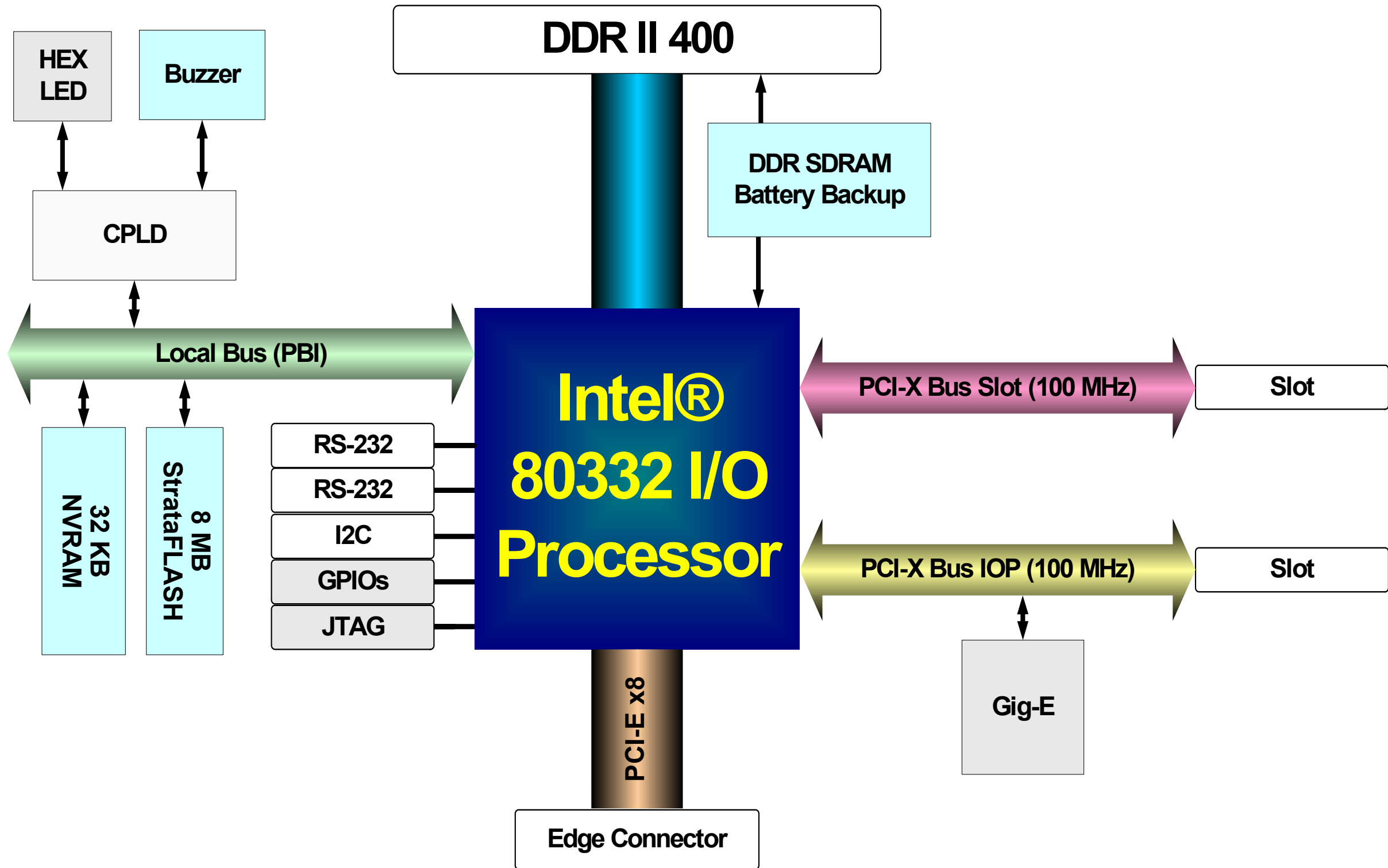
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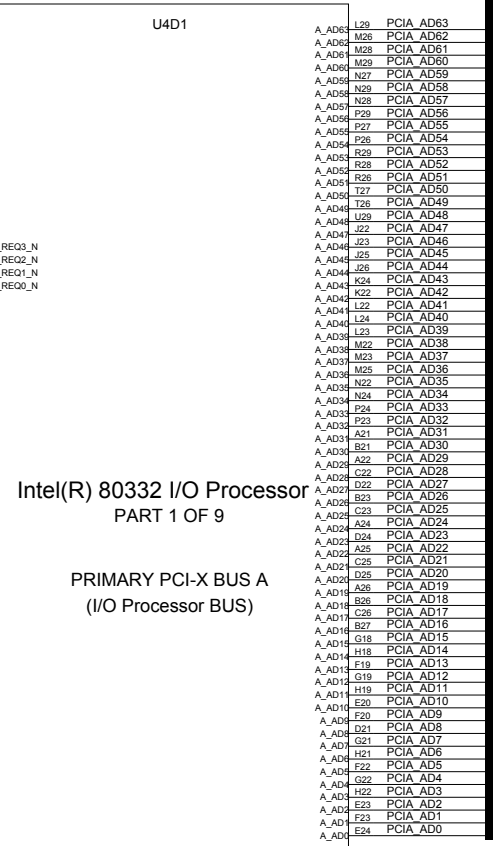
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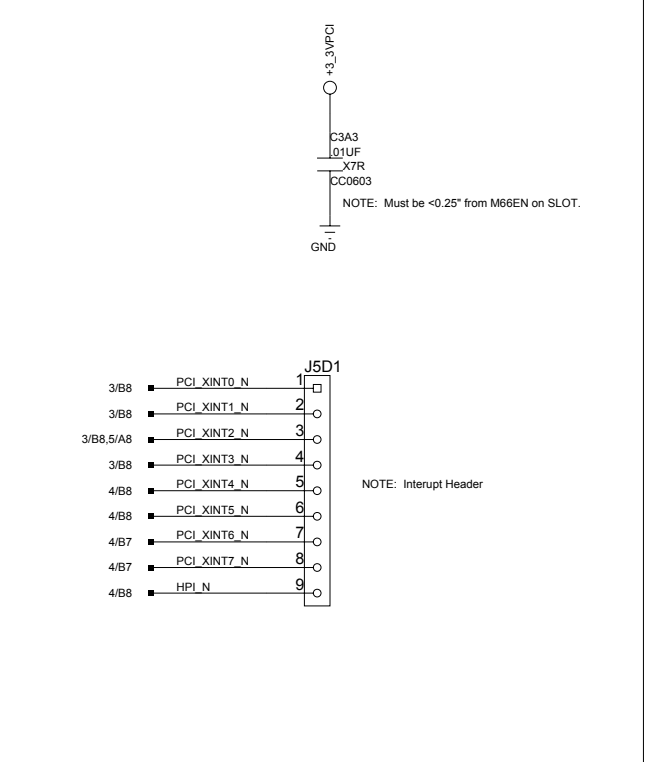
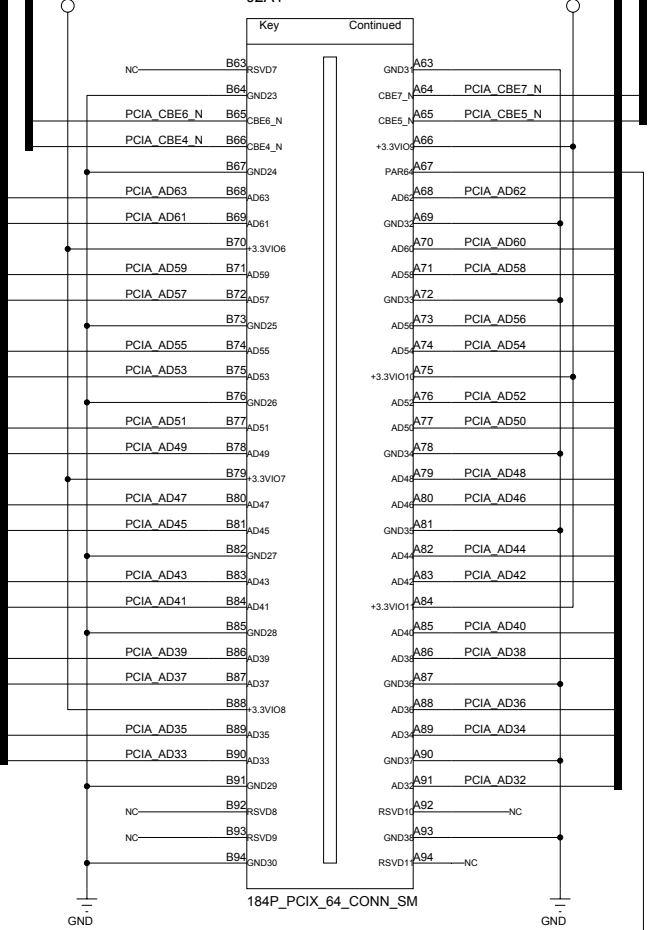
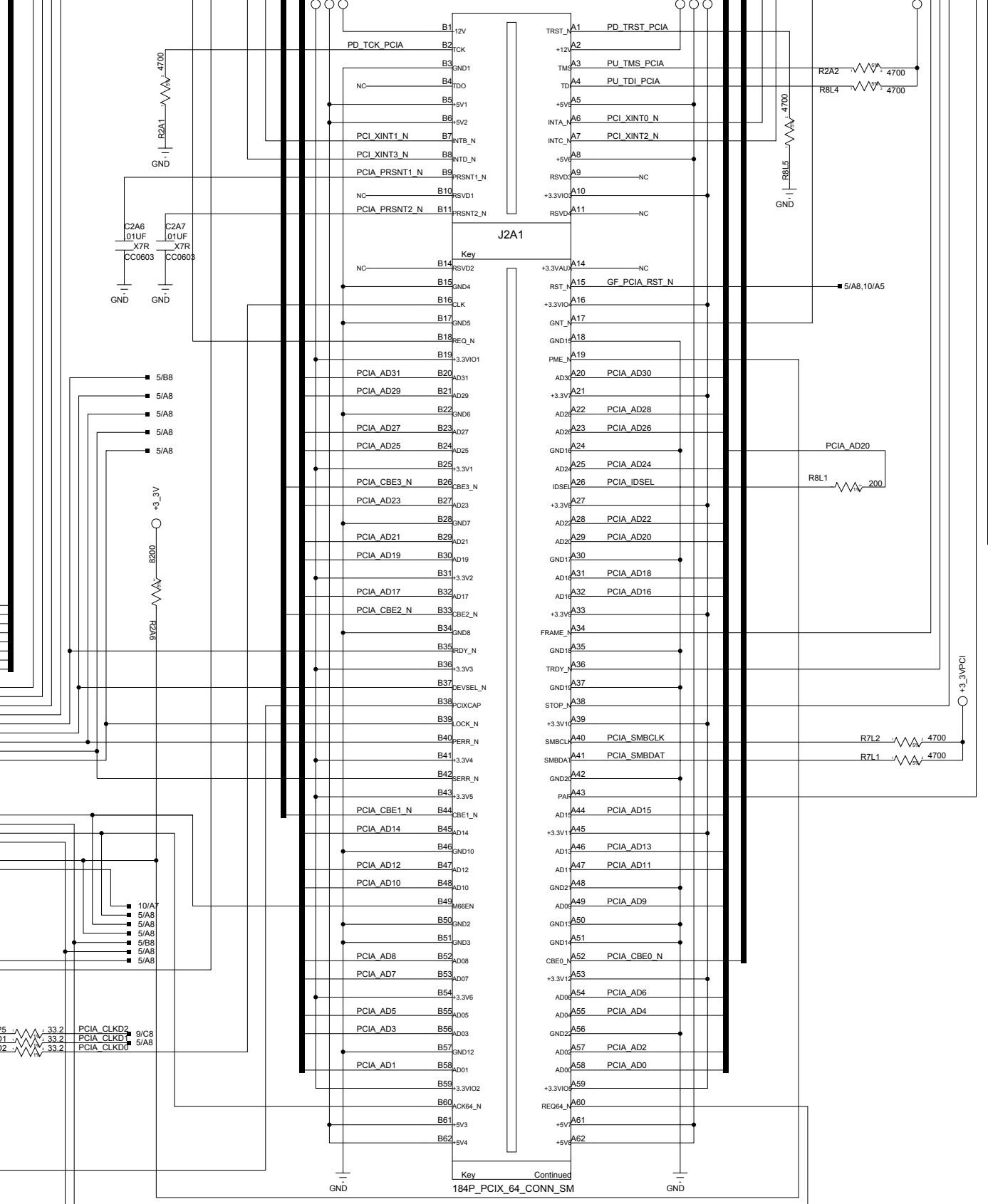
P1

INTEL(R) IQ80332 BLOCK DIAGRAM

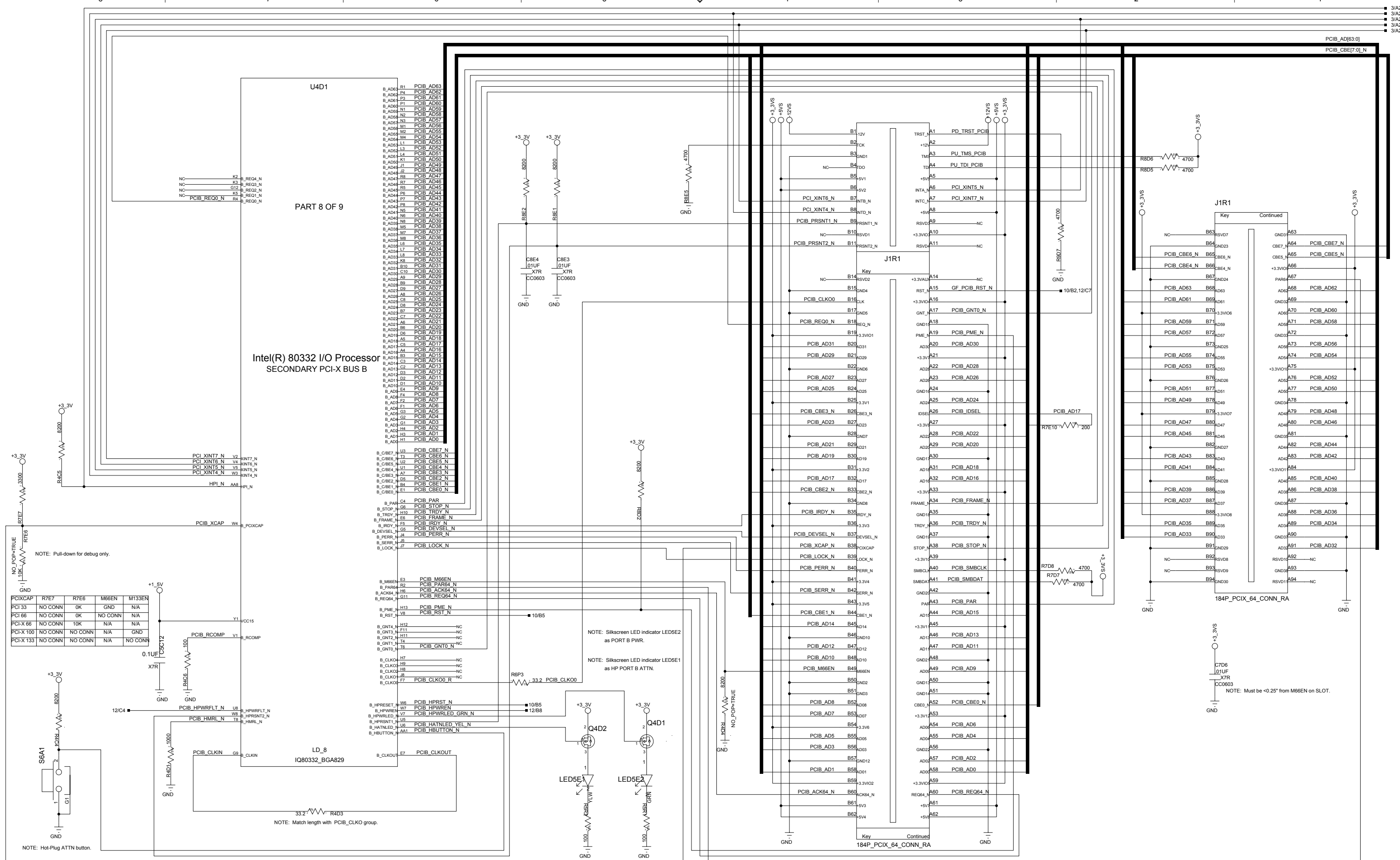




A_AD63	L29	PCIA AD63
A_AD62	M28	PCIA AD62
A_AD61	M29	PCIA AD61
A_AD60	M29	PCIA AD60
A_AD59	N27	PCIA AD59
A_AD58	N29	PCIA AD58
A_AD57	N28	PCIA AD57
A_AD56	P29	PCIA AD56
A_AD55	P27	PCIA AD55
A_AD54	F28	PCIA AD54
A_AD53	K29	PCIA AD53
A_AD52	R28	PCIA AD52
A_AD51	R28	PCIA AD51
A_AD50	T27	PCIA AD50
A_AD49	U29	PCIA AD49
A_AD48	U29	PCIA AD48
A_AD47	J22	PCIA AD47
A_AD46	J23	PCIA AD46
A_AD45	J24	PCIA AD45
A_AD44	J25	PCIA AD44
A_AD43	K24	PCIA AD43
A_AD42	K22	PCIA AD42
A_AD41	L22	PCIA AD41
A_AD40	L24	PCIA AD40
A_AD39	L23	PCIA AD39
A_AD38	M22	PCIA AD38
A_AD37	M23	PCIA AD37
A_AD36	M25	PCIA AD36
A_AD35	N22	PCIA AD35
A_AD34	N24	PCIA AD34
A_AD33	P24	PCIA AD33
A_AD32	P23	PCIA AD32
A_AD31	A21	PCIA AD31
A_AD30	B21	PCIA AD30
A_AD29	A22	PCIA AD29
A_AD28	D22	PCIA AD28
A_AD27	D22	PCIA AD27
A_AD26	B23	PCIA AD26
A_AD25	C23	PCIA AD25
A_AD24	A24	PCIA AD24
A_AD23	B24	PCIA AD23
A_AD22	A25	PCIA AD22
A_AD21	C25	PCIA AD21
A_AD20	D25	PCIA AD20
A_AD19	A26	PCIA AD19
A_AD18	B26	PCIA AD18
A_AD17	C26	PCIA AD17
A_AD16	B27	PCIA AD16
A_AD15	G18	PCIA AD15
A_AD14	H18	PCIA AD14
A_AD13	F19	PCIA AD13
A_AD12	G19	PCIA AD12
A_AD11	H19	PCIA AD11
A_AD10	E20	PCIA AD10
A_AD9	F20	PCIA AD9
A_AD8	D21	PCIA AD8
A_AD7	G21	PCIA AD7
A_AD6	H21	PCIA AD6
A_AD5	F22	PCIA AD5
A_AD4	G22	PCIA AD4
A_AD3	H22	PCIA AD3
A_AD2	E23	PCIA AD2
A_AD1	F23	PCIA AD1
A_AD0	E24	PCIA AD0
A_CBET_N	L27	PCIA CBET N
A_CBE6_N	L28	PCIA CBE6 N
A_CBE5_N	K28	PCIA CBE5 N
A_CBE4_N	K27	PCIA CBE4 N
A_CBE3_N	L27	PCIA CBE3 N
A_CBE2_N	L27	PCIA CBE2 N
A_CBE1_N	H17	PCIA CBE1 N
A_CBE0_N	H20	PCIA CBE0 N
A_PAR	F26	PCIA PAR
A_STOP_N	D28	PCIA STOP N
A_TRDY_N	E28	PCIA TRDY N
A_FRAME_N	C28	PCIA FRAME N
A_IRDY_N	E29	PCIA IRDY N
A_DEVSEL_N	F29	PCIA DEVSEL N
A_PERR_N	G29	PCIA PERR N
A_SERR_N	E26	PCIA SERR N
A_LOCK_N	E27	PCIA LOCK N
A_M66EN	C20	PCIA M66EN
A_PAR64	K29	PCIA PAR64
A_ACK64_N	J28	PCIA ACK64 N
A_REQ64_N	J29	PCIA REQ64 N
A_PME_N	R25	PCIA PME N
A_RST_N	R22	PCIA RST N
A_GNT3_N	U25	NC
A_GNT2_N	P22	NC
A_GNT1_N	B24	PCIA GNT1 N
A_GNT0_N	A23	PCIA GNT0 N
A_CLKO2	H23	PCIA CLKD2 R R7P5
A_CLKO1	G24	PCIA CLKD1 R R3D1
A_CLKO0	H24	PCIA CLKD0 R R3D2
A_CLKOUT	G25	PCIA CLKOUT



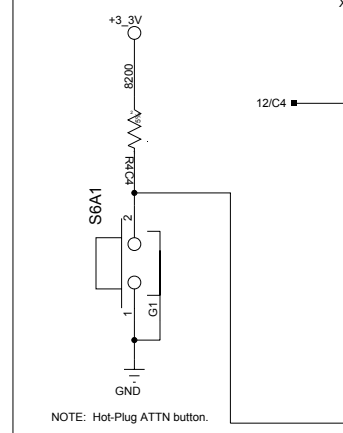
PCI-A BUS



U4D1
PART 8 OF 9
Intel(R) 80332 I/O Processor
SECONDARY PCI-X BUS B

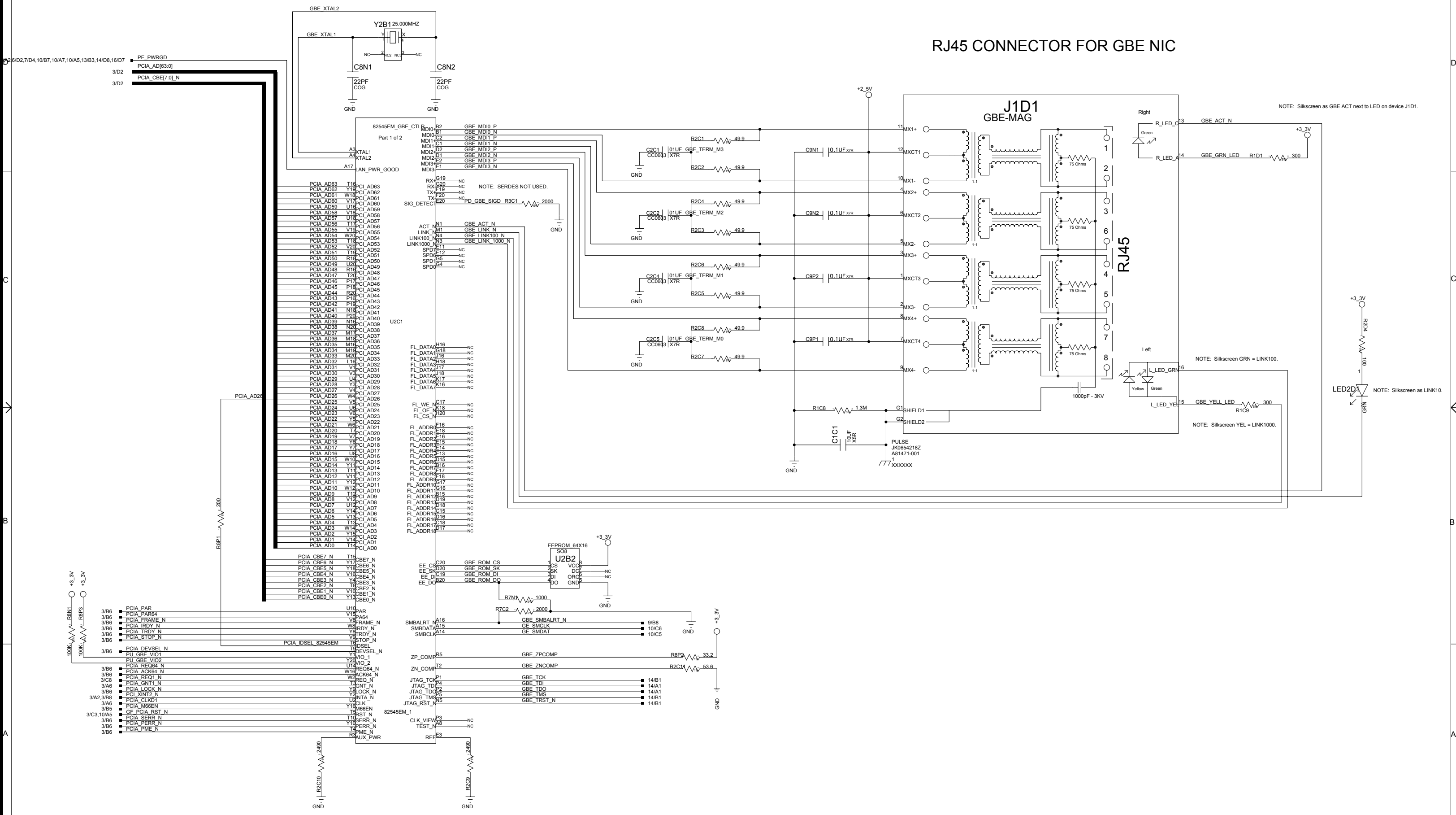
- B_AD63 R1 PCIB AD63
- B_AD62 R2 PCIB AD62
- B_AD61 R3 PCIB AD61
- B_AD60 P1 PCIB AD60
- B_AD59 N1 PCIB AD59
- B_AD58 N2 PCIB AD58
- B_AD57 N3 PCIB AD57
- B_AD56 M1 PCIB AD56
- B_AD55 M2 PCIB AD55
- B_AD54 M4 PCIB AD54
- B_AD53 L1 PCIB AD53
- B_AD52 L3 PCIB AD52
- B_AD51 L4 PCIB AD51
- B_AD50 M4 PCIB AD50
- B_AD49 J1 PCIB AD49
- B_AD48 J2 PCIB AD48
- B_AD47 R8 PCIB AD47
- B_AD46 R7 PCIB AD46
- B_AD45 R5 PCIB AD45
- B_AD44 R6 PCIB AD44
- B_AD43 P7 PCIB AD43
- B_AD42 P8 PCIB AD42
- B_AD41 N5 PCIB AD41
- B_AD40 N6 PCIB AD40
- B_AD39 N8 PCIB AD39
- B_AD38 M5 PCIB AD38
- B_AD37 M7 PCIB AD37
- B_AD36 M8 PCIB AD36
- B_AD35 L6 PCIB AD35
- B_AD34 L7 PCIB AD34
- B_AD33 L8 PCIB AD33
- B_AD32 K8 PCIB AD32
- B_AD31 K9 PCIB AD31
- B_AD30 C10 PCIB AD30
- B_AD29 A9 PCIB AD29
- B_AD28 B9 PCIB AD28
- B_AD27 D9 PCIB AD27
- B_AD26 A8 PCIB AD26
- B_AD25 C8 PCIB AD25
- B_AD24 D8 PCIB AD24
- B_AD23 B7 PCIB AD23
- B_AD22 C7 PCIB AD22
- B_AD21 B6 PCIB AD21
- B_AD20 D6 PCIB AD20
- B_AD19 D5 PCIB AD19
- B_AD18 A5 PCIB AD18
- B_AD17 C5 PCIB AD17
- B_AD16 A4 PCIB AD16
- B_AD15 B3 PCIB AD15
- B_AD14 C3 PCIB AD14
- B_AD13 D3 PCIB AD13
- B_AD12 B2 PCIB AD12
- B_AD11 D2 PCIB AD11
- B_AD10 D1 PCIB AD10
- B_AD9 E4 PCIB AD9
- B_AD8 F4 PCIB AD8
- B_AD7 F2 PCIB AD7
- B_AD6 F1 PCIB AD6
- B_AD5 G3 PCIB AD5
- B_AD4 C2 PCIB AD4
- B_AD3 G1 PCIB AD3
- B_AD2 H4 PCIB AD2
- B_AD1 H3 PCIB AD1
- B_AD0 H1 PCIB AD0
- B_CBE7_N U3 PCIB CBE7 N
- B_CBE6_N T3 PCIB CBE6 N
- B_CBE5_N U2 PCIB CBE5 N
- B_CBE4_N L1 PCIB CBE4 N
- B_CBE3_N A7 PCIB CBE3 N
- B_CBE2_N D5 PCIB CBE2 N
- B_CBE1_N B4 PCIB CBE1 N
- B_CBE0_N E1 PCIB CBE0 N
- B_PAR C4 PCIB PAR
- B_STOP_G6 PCIB STOP N
- B_TRDY_H10 PCIB TRDY N
- B_FRAME_E8 PCIB FRAME N
- B_IRDY_F5 PCIB IRDY N
- B_DEVSEL_G5 PCIB DEVSEL N
- B_PERR_J4 PCIB PERR N
- B_SERR_J5 PCIB SERR N
- B_LOCK_J7 PCIB LOCK N
- B_M66EN E3 PCIB M66EN
- B_PAR64_R2 PCIB PAR64 N
- B_ACK64_H6 PCIB ACK64 N
- B_REQ64_G11 PCIB REQ64 N
- B_PME_H13 PCIB PME N
- B_RST_V8 PCIB RST N
- B_GNT4_H12 NC
- B_GNT3_H11 NC
- B_GNT2_T4 NC
- B_GNT1_T6 PCIB GNT0 N
- B_CLKO_H7 NC
- B_CLKO_H9 NC
- B_CLKO_H8 NC
- B_CLKO_J8 PCIB CLK00 R
- B_HPRST_W8 PCIB HPRST N
- B_HPWRN_W7 PCIB HPWRN N
- B_HPWRLED_V7 PCIB HPWRLED GRN N
- B_HPRST1_U5 PCIB HPRST1 N
- B_HATNLED_U8 PCIB HATNLED YEL N
- B_HBUTTON_A41 PCIB HBUTTON N
- B_CLKIN_G8 PCIB CLKIN
- B_CLKOUT_E7 PCIB CLKOUT

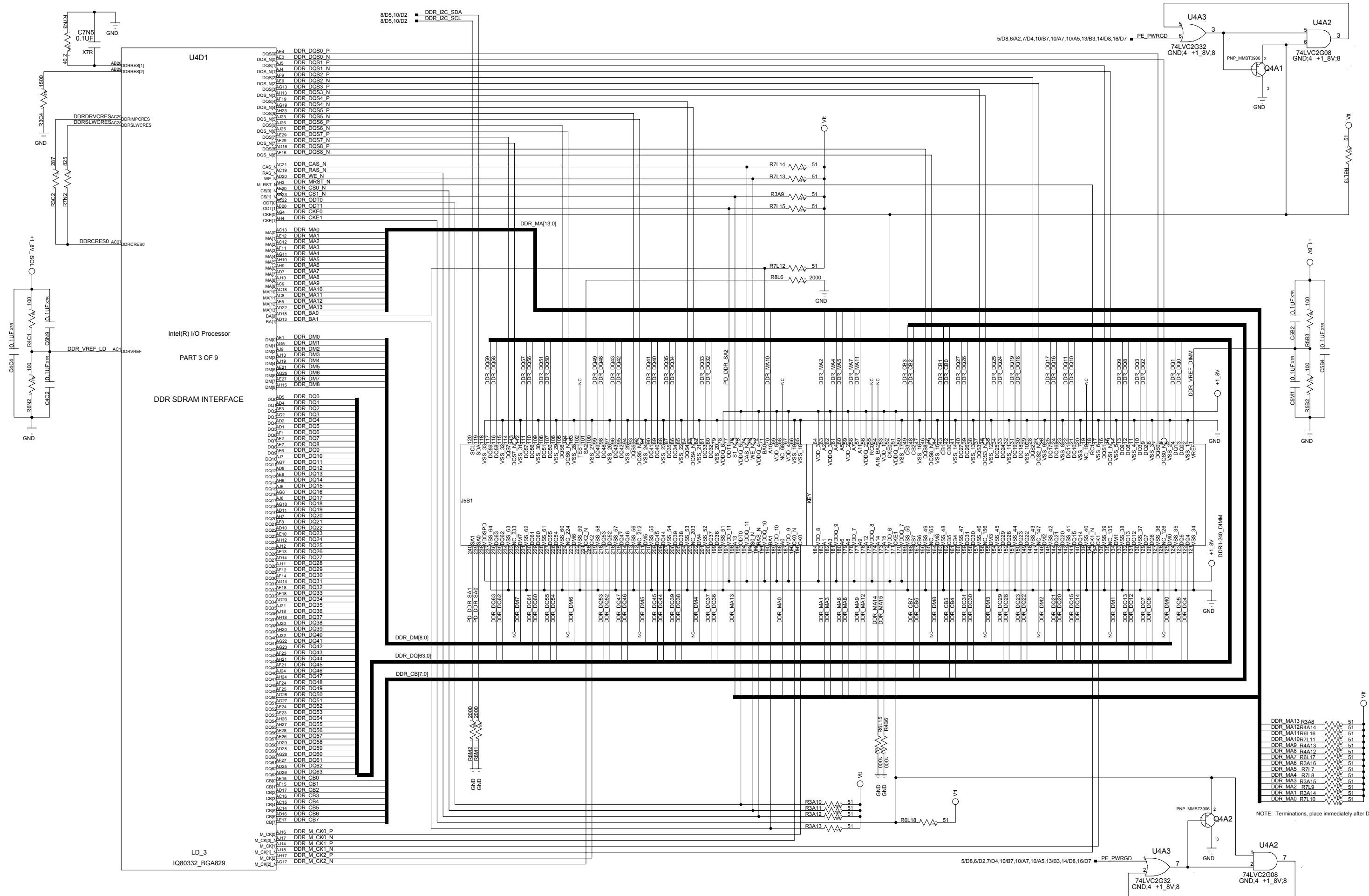
PCIXCAP	R7E7	R7E6	M66EN	M133EN
PCI 33	NO CONN	OK	GND	N/A
PCI 66	NO CONN	OK	NO CONN	N/A
PCI-X 66	NO CONN	10K	N/A	N/A
PCI-X 100	NO CONN	NO CONN	N/A	GND
PCI-X 133	NO CONN	NO CONN	N/A	NO CONN

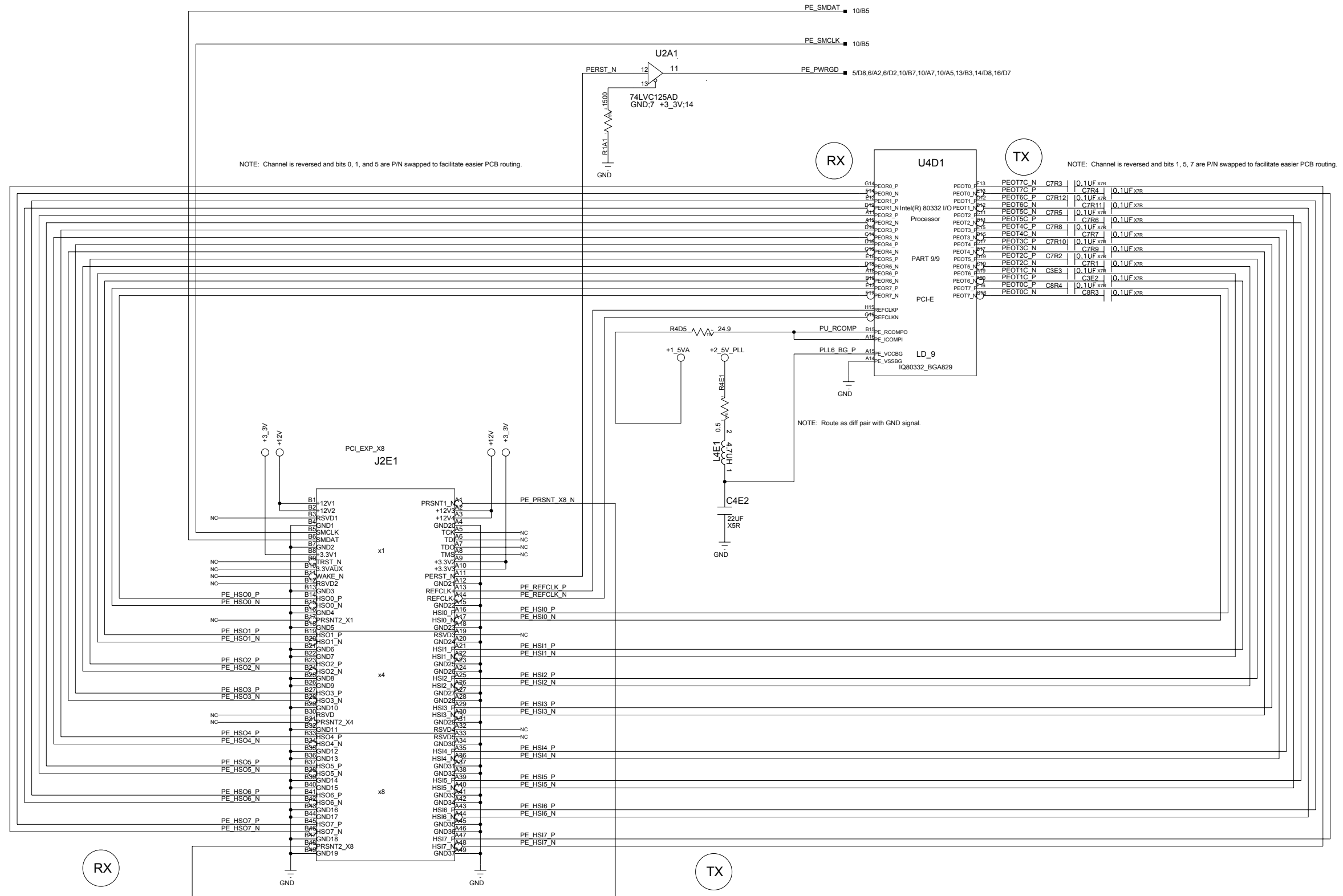


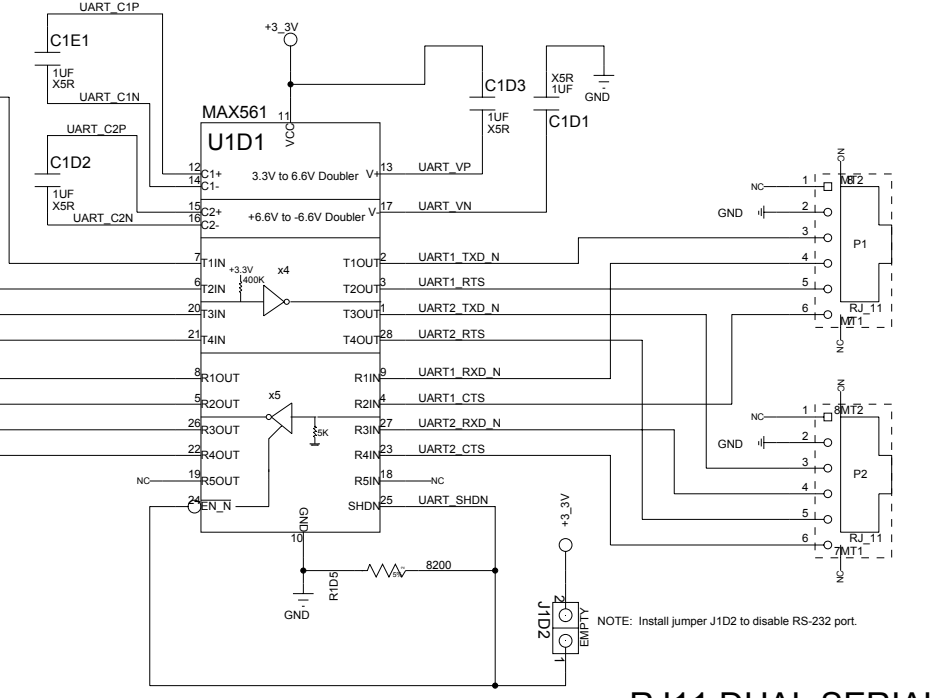
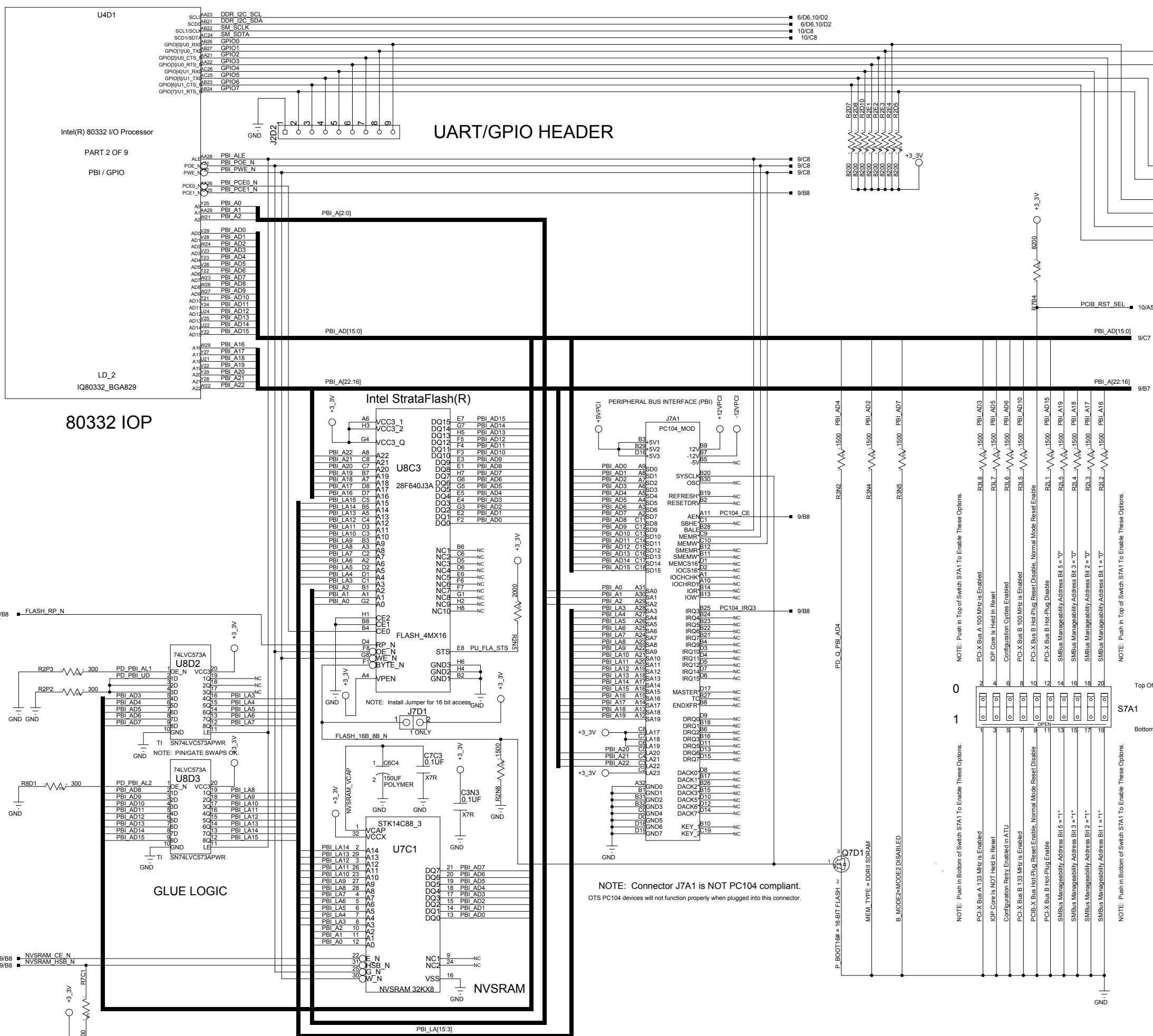
GBE CONTROLLER

RJ45 CONNECTOR FOR GBE NIC









RS-232 TRANSCEIVER

RJ11 DUAL SERIAL PORT CONNECTOR

SWITCH S7A1

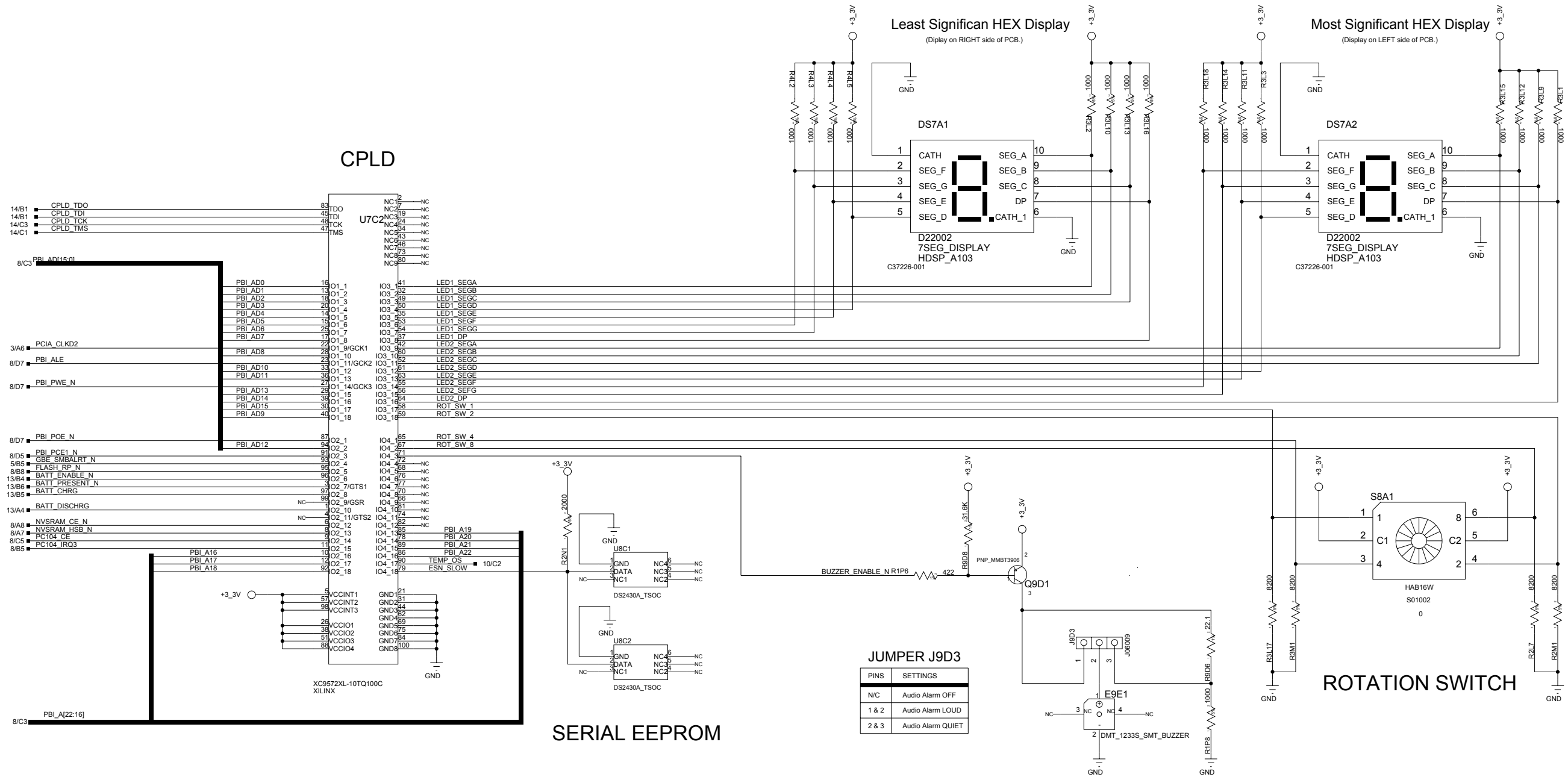
S7A1 SWITCH #	SIGNAL NAME	SWITCH SETTING	SIGNAL VALUE	STRAPPING DESCRIPTION
1	PBI_AD3	* PUSHED IN AT THE TOP	0	PCI-X Bus A 100 Mhz is Enabled.
		PUSHED IN AT THE BOTTOM	1	PCI-X Bus A 133 Mhz is Enabled
2	PBI_AD5	PUSHED IN AT THE TOP	0	IOP Core is Held In Reset
		* PUSHED IN AT THE BOTTOM	1	IOP Core is NOT Held In Reset
3	PBI_AD6	PUSHED IN AT THE TOP	0	Configuration Cycles Enabled - use when booting in a passive backplane
		* PUSHED IN AT THE BOTTOM	1	Configuration Retry Enabled in ATU - use when booting in a host
4	PBI_AD10	* PUSHED IN AT THE TOP	0	PCI-X Bus B 100 Mhz is Enabled
		PUSHED IN AT THE BOTTOM	1	PCI-X Bus B 133 Mhz is Enabled
5	PBI_AD11	* PUSHED IN AT THE TOP	0	PCI-X Bus B Hot-Plug Reset Disable, PCI-X Bus B Normal Mode Reset Enable
		PUSHED IN AT THE BOTTOM	1	PCI-X Bus B Hot-Plug Reset Enable, PCI-X Bus B Normal Mode Reset Disable
6	PBI_AD15	* PUSHED IN AT THE TOP	0	PCI-X Bus B Hot-Plug Disable
		PUSHED IN AT THE BOTTOM	1	PCI-X Bus B Hot-Plug Enable
7	PBI_A19	PUSHED IN AT THE TOP	0	SMBus Manageability Address Bit 5 = "0"
		* PUSHED IN AT THE BOTTOM	1	SMBus Manageability Address Bit 5 = "1"
8	PBI_A18	PUSHED IN AT THE TOP	0	SMBus Manageability Address Bit 3 = "0"
		* PUSHED IN AT THE BOTTOM	1	SMBus Manageability Address Bit 3 = "1"
9	PBI_A17	PUSHED IN AT THE TOP	0	SMBus Manageability Address Bit 2 = "0"
		* PUSHED IN AT THE BOTTOM	1	SMBus Manageability Address Bit 2 = "1"
10	PBI_A16	PUSHED IN AT THE TOP	0	SMBus Manageability Address Bit 1 = "0"
		* PUSHED IN AT THE BOTTOM	1	SMBus Manageability Address Bit 1 = "1"

* Default switch settings

PBI / FLASH / NVSRAM / UART TX-RX / BOOT STRAPPINGS

HEX DISPLAYS

NOTE: When running RedBoot, a proper boot results with an output of A1 on the hex display.
 NOTE: When core is held in reset (default setting), no output results on the hex display.



Least Significant HEX Display
(Display on RIGHT side of PCB.)

Most Significant HEX Display
(Display on LEFT side of PCB.)

SERIAL EEPROM

JUMPER J9D3

PINS	SETTINGS
N/C	Audio Alarm OFF
1 & 2	Audio Alarm LOUD
2 & 3	Audio Alarm QUIET

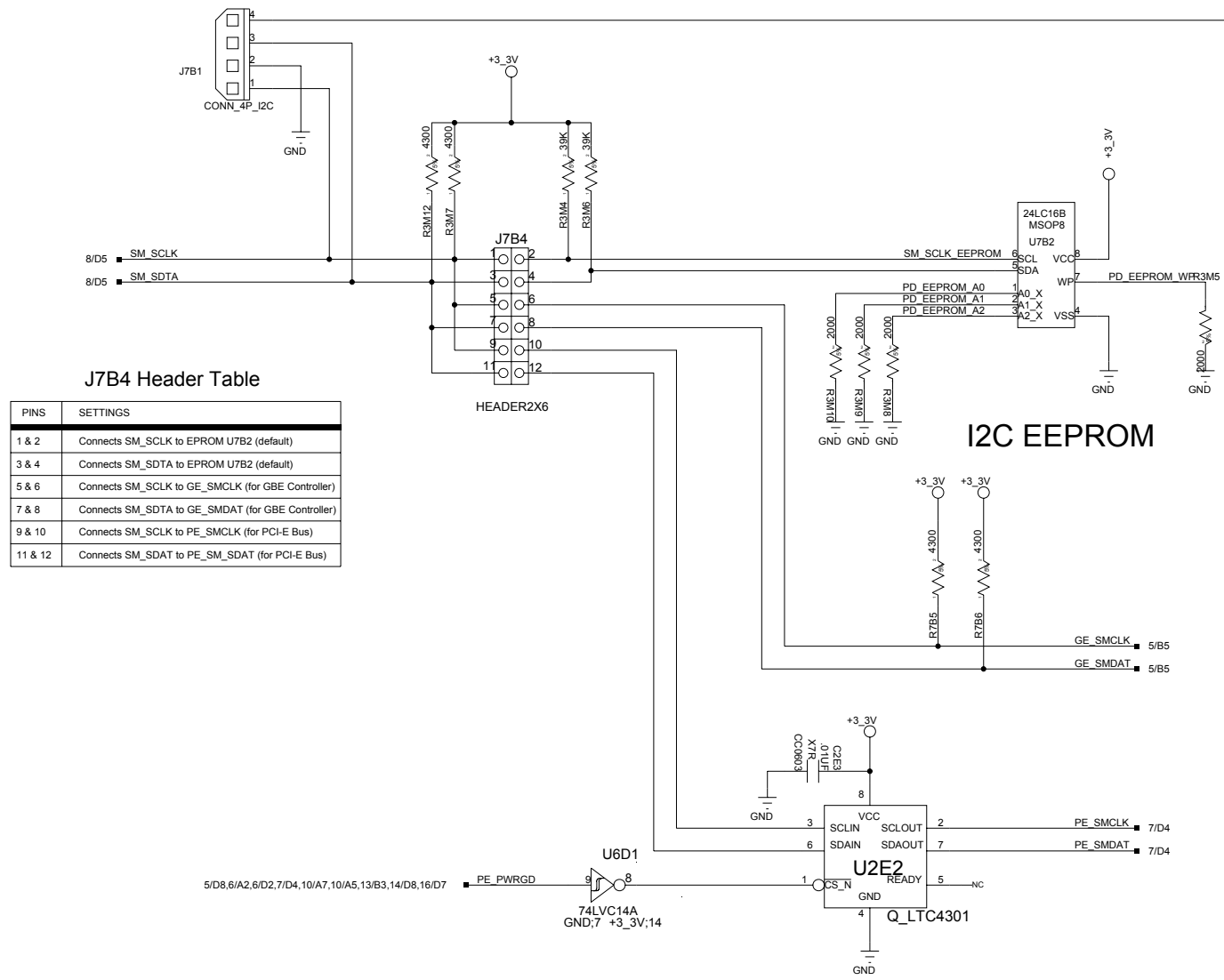
AUDIO ALARM

ROTATION SWITCH

SWITCH S8A1

POSITION	SETTINGS
0	Enable Private Devices on the Secondary PCI bus - allows RedBoot to configure and use devices in Slot A
1	Disable Private Devices on the Secondary PCI bus - allows the host to see all devices on secondary PCI bus
2 - F	N/A - dependent upon firmware and/or software utilization

I2C EPROM HEADER



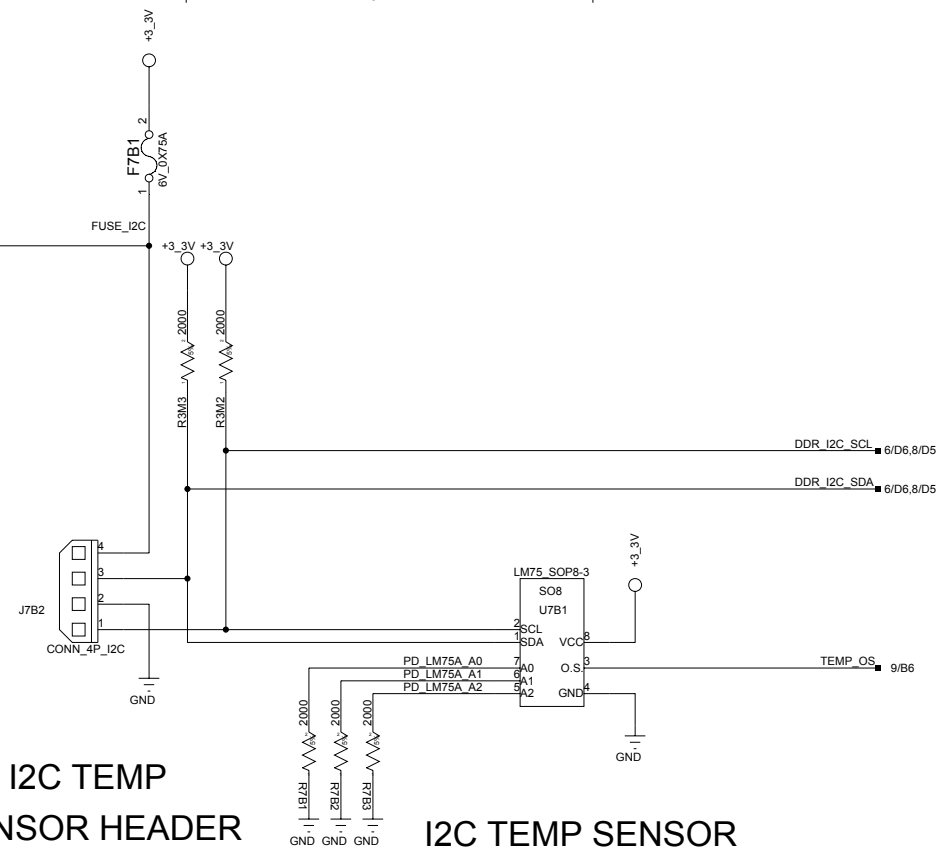
J7B4 Header Table

PINS	SETTINGS
1 & 2	Connects SM_SCLK to EPROM U7B2 (default)
3 & 4	Connects SM_SDTA to EPROM U7B2 (default)
5 & 6	Connects SM_SCLK to GE_SMCLK (for GBE Controller)
7 & 8	Connects SM_SDTA to GE_SMDAT (for GBE Controller)
9 & 10	Connects SM_SCLK to PE_SMCLK (for PCI-E Bus)
11 & 12	Connects SM_SDAT to PE_SM_DAT (for PCI-E Bus)

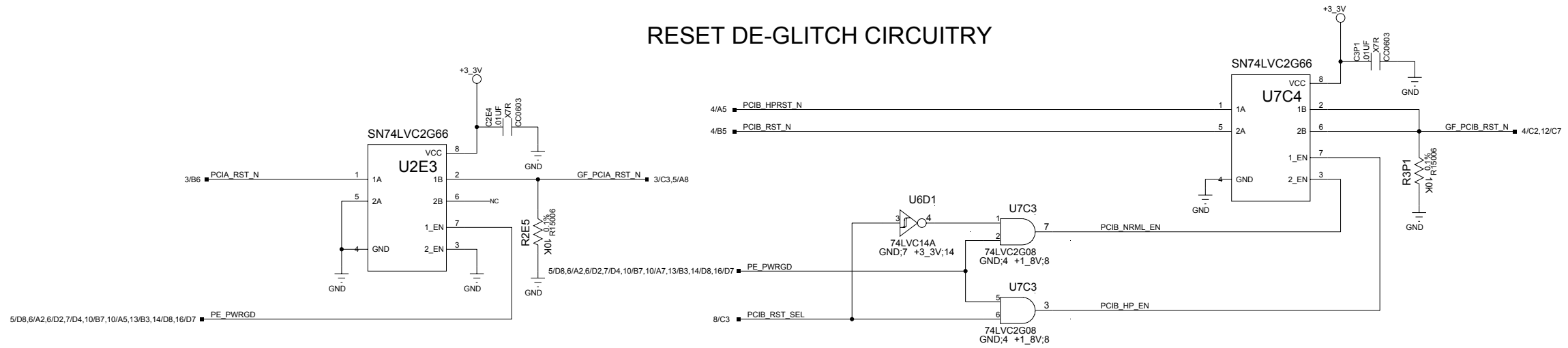
I2C EEPROM

I2C TEMP SENSOR HEADER

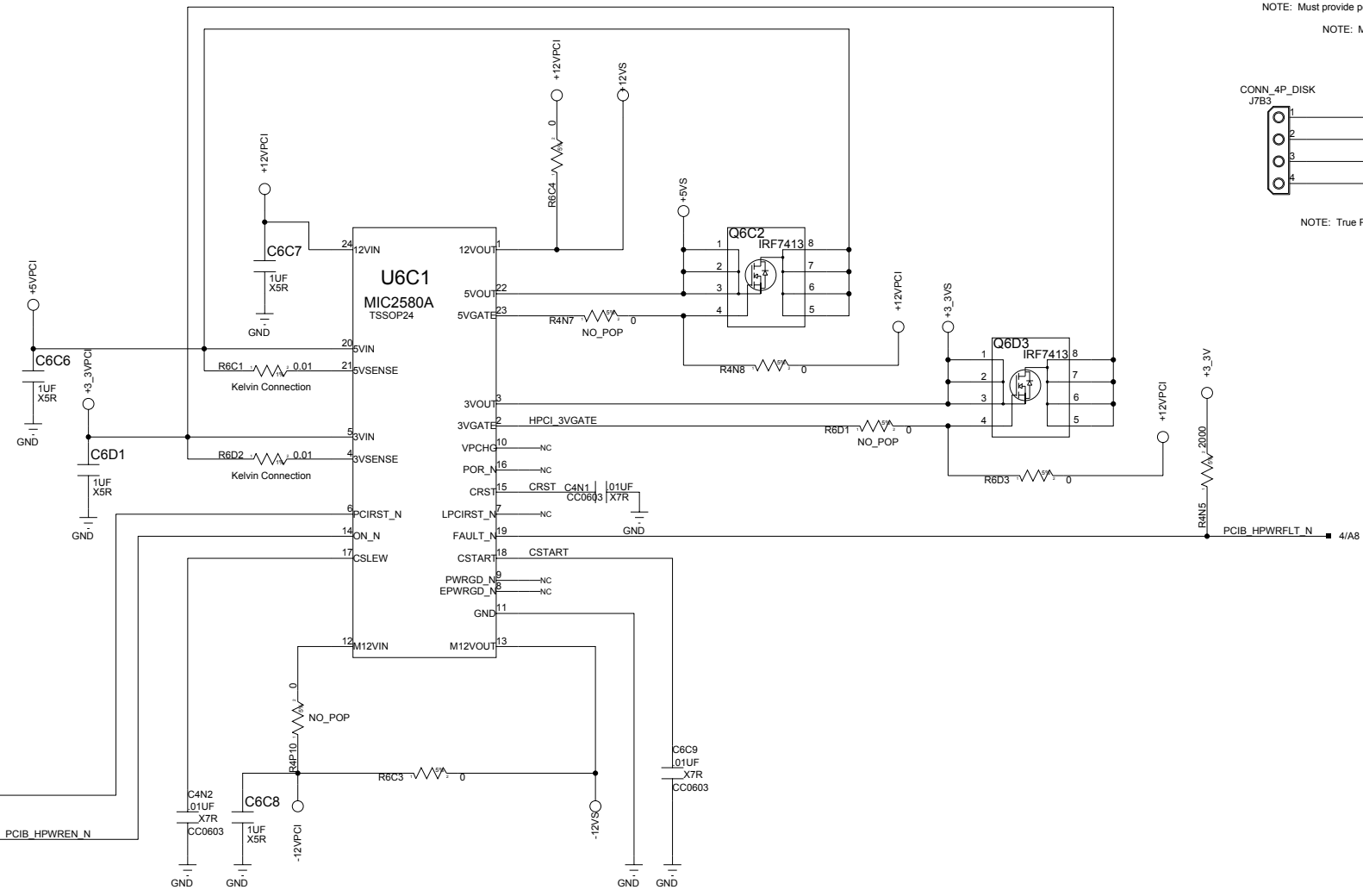
I2C TEMP SENSOR



RESET DE-GLITCH CIRCUITRY



Secondary PCI B-Slot Hot-Plug Power Controller



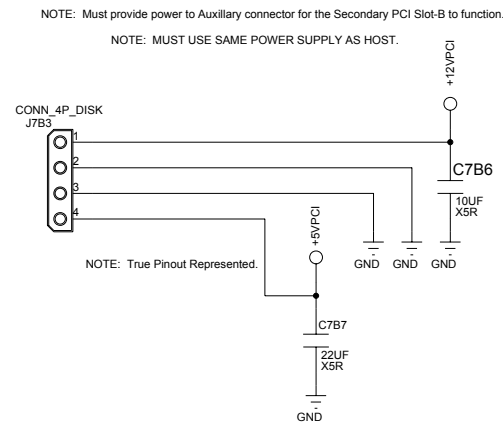
NOTE: Hot-Plug capability requires an additional parts kit.

NOTE: Must have BIOS support in order for Hot-Plug to function properly.

* PCI B-Slot Normal Operation		PCI B-Slot Hot-Plug Operation	
POPULATE	NO-POP	POPULATE	NO-POP
R6C4	R4N7	R4N7	R6C4
R4N8	R6D1	R6D1	R4N8
R6D3	R4P10	R4P10	R6D3
R6C3	J7C1 Device	J7C1 Device	R6C3

* Default setting

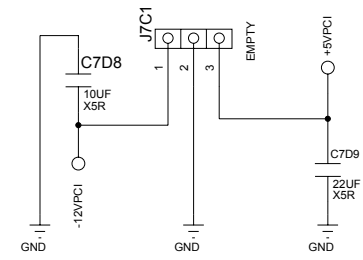
AUX POWER SUPPLY



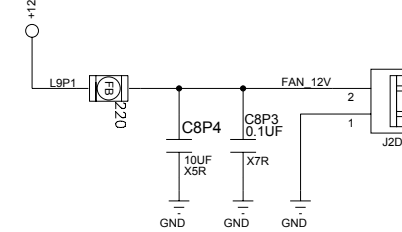
NOTE: True Pinout Represented.

-12V Buck-Boost Regulator Socket

NOTE: Facilitates regulator from Hot-Plug capability kit.

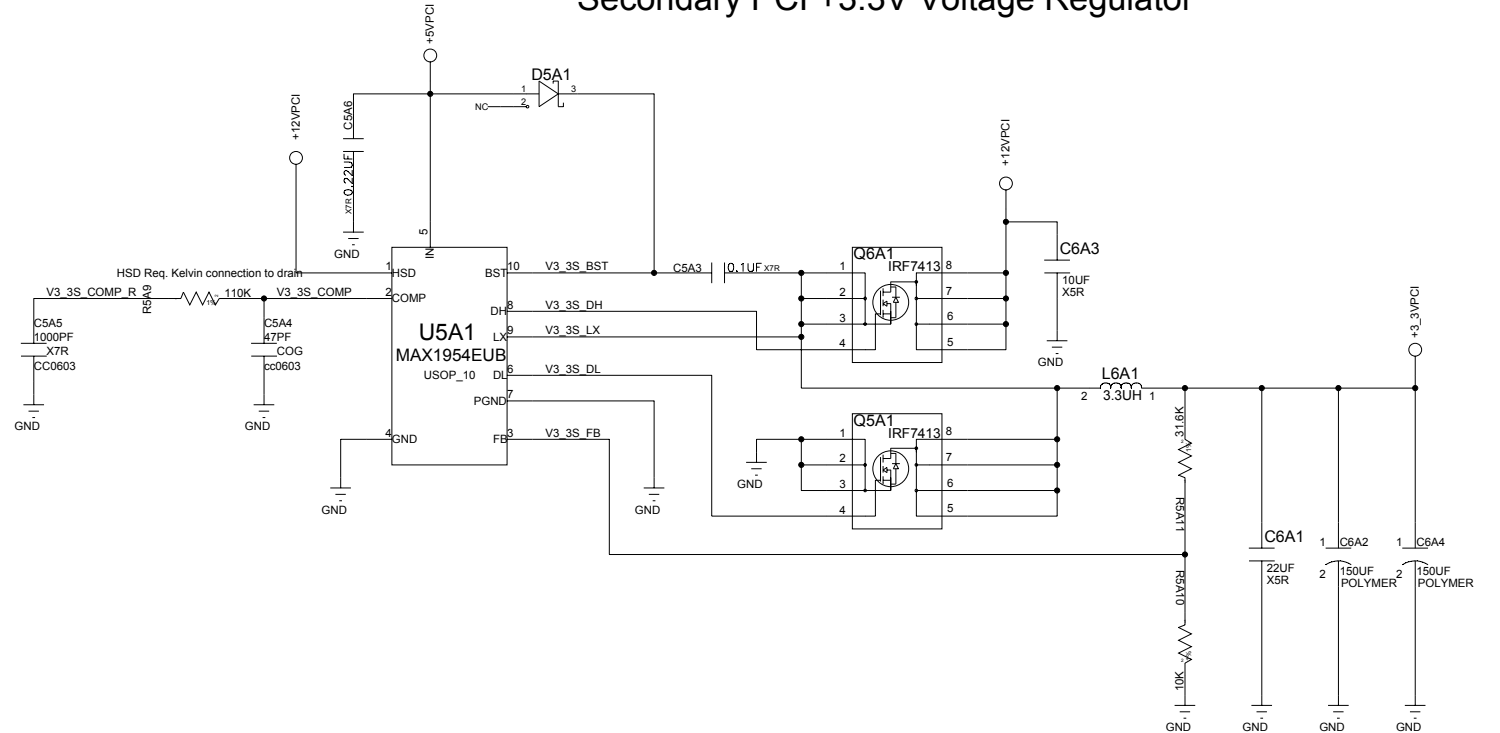


FAN POWER HEADER

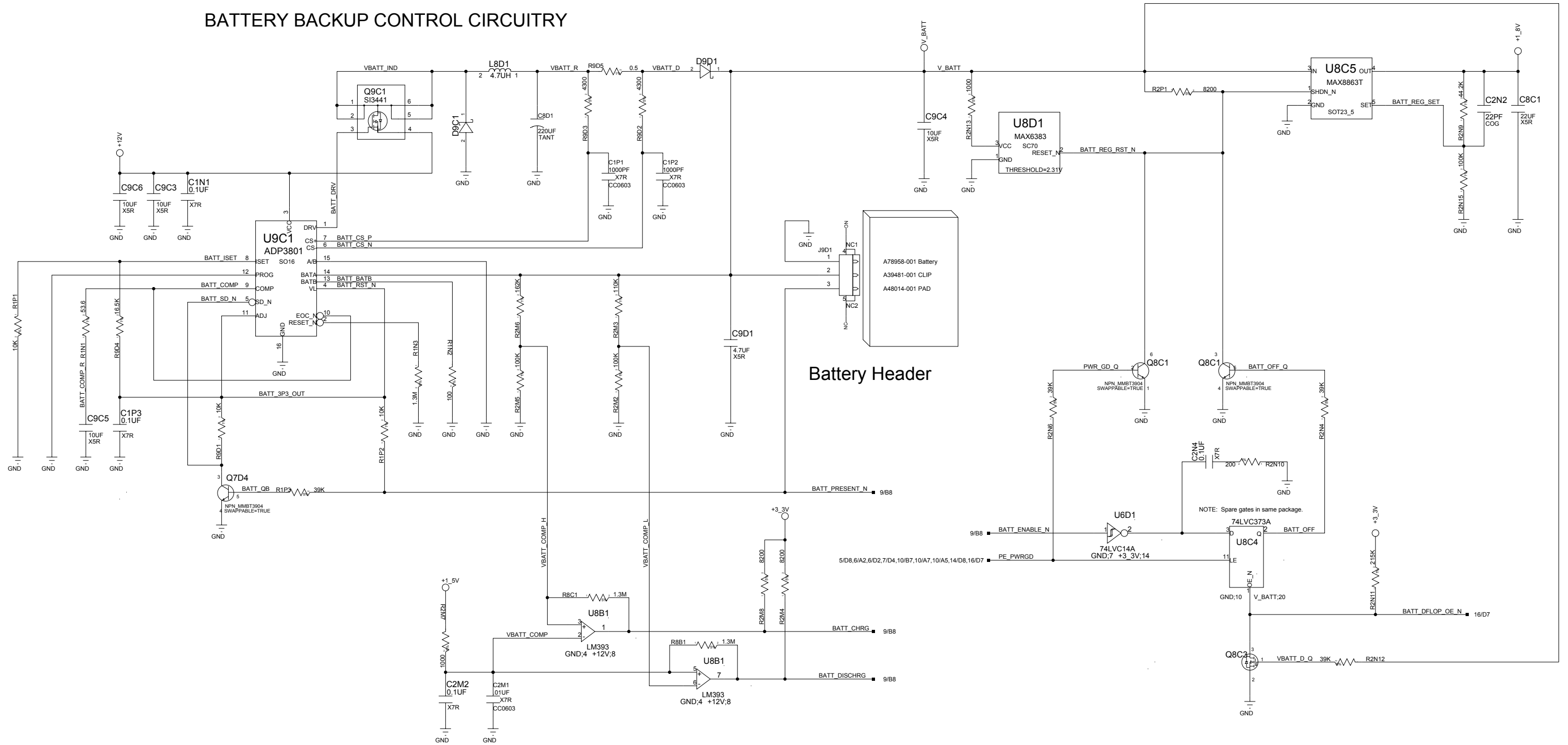


NOTE:
Header J2D1 is to be utilized for active IOP cooling.
The active heat sink part number is: C51629-001.
The passive IOP cooling solution requires at least 200 lfm across its surface.
The passive heat sink part number is: C50161-001.

Secondary PCI +3.3V Voltage Regulator



BATTERY BACKUP CONTROL CIRCUITRY



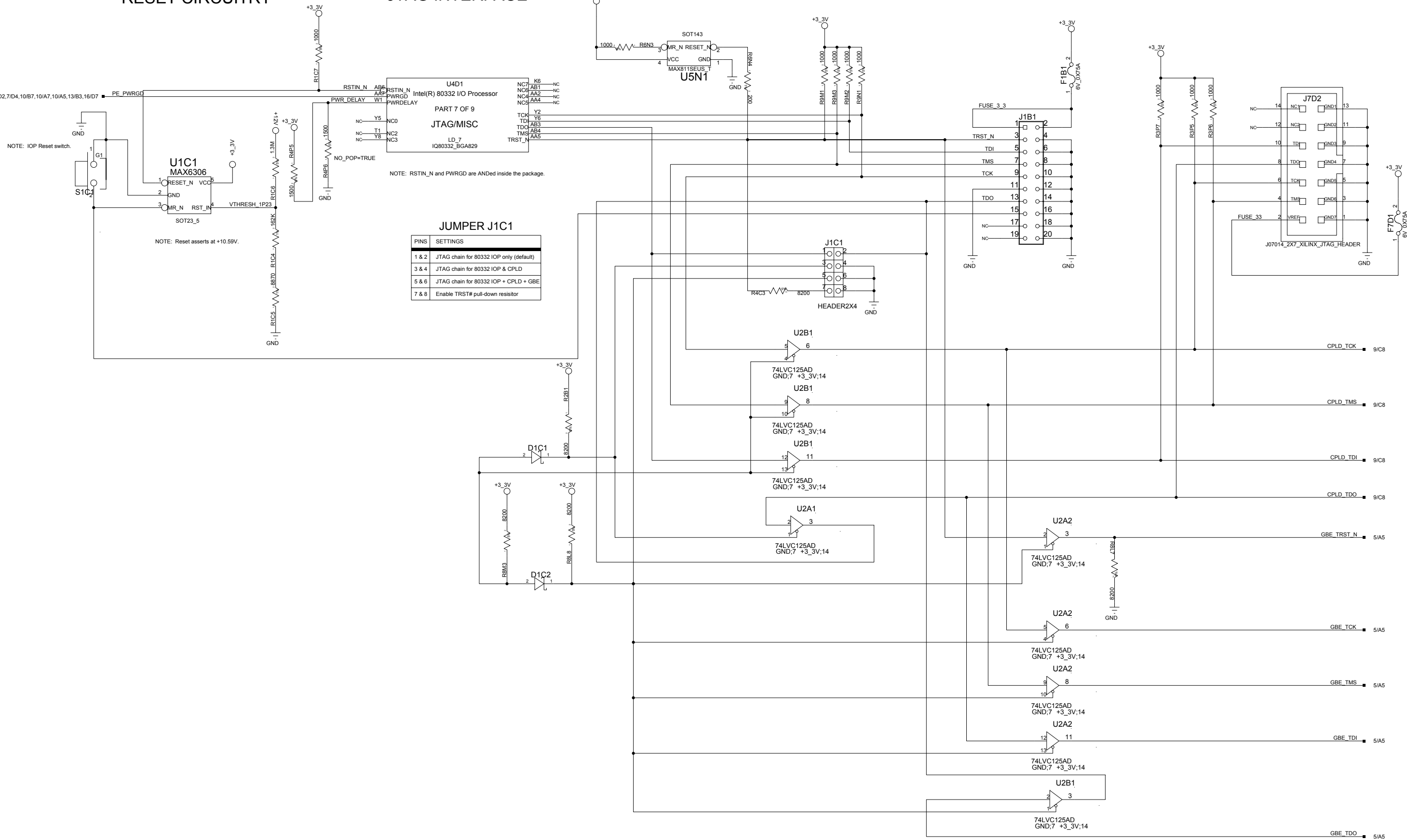
DDR SELF-REFRESH LINEAR REGULATOR

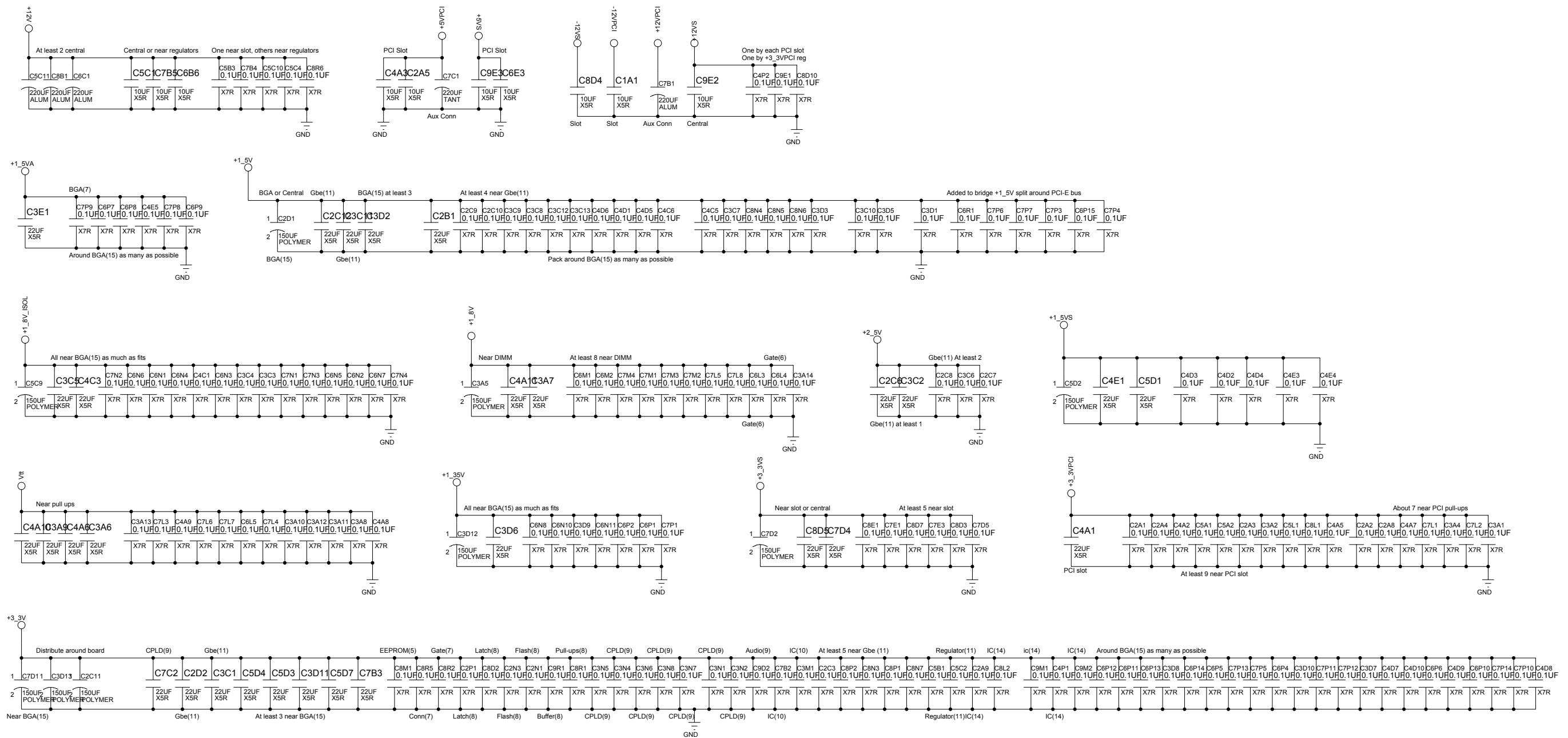
RESET CIRCUITRY

JTAG INTERFACE

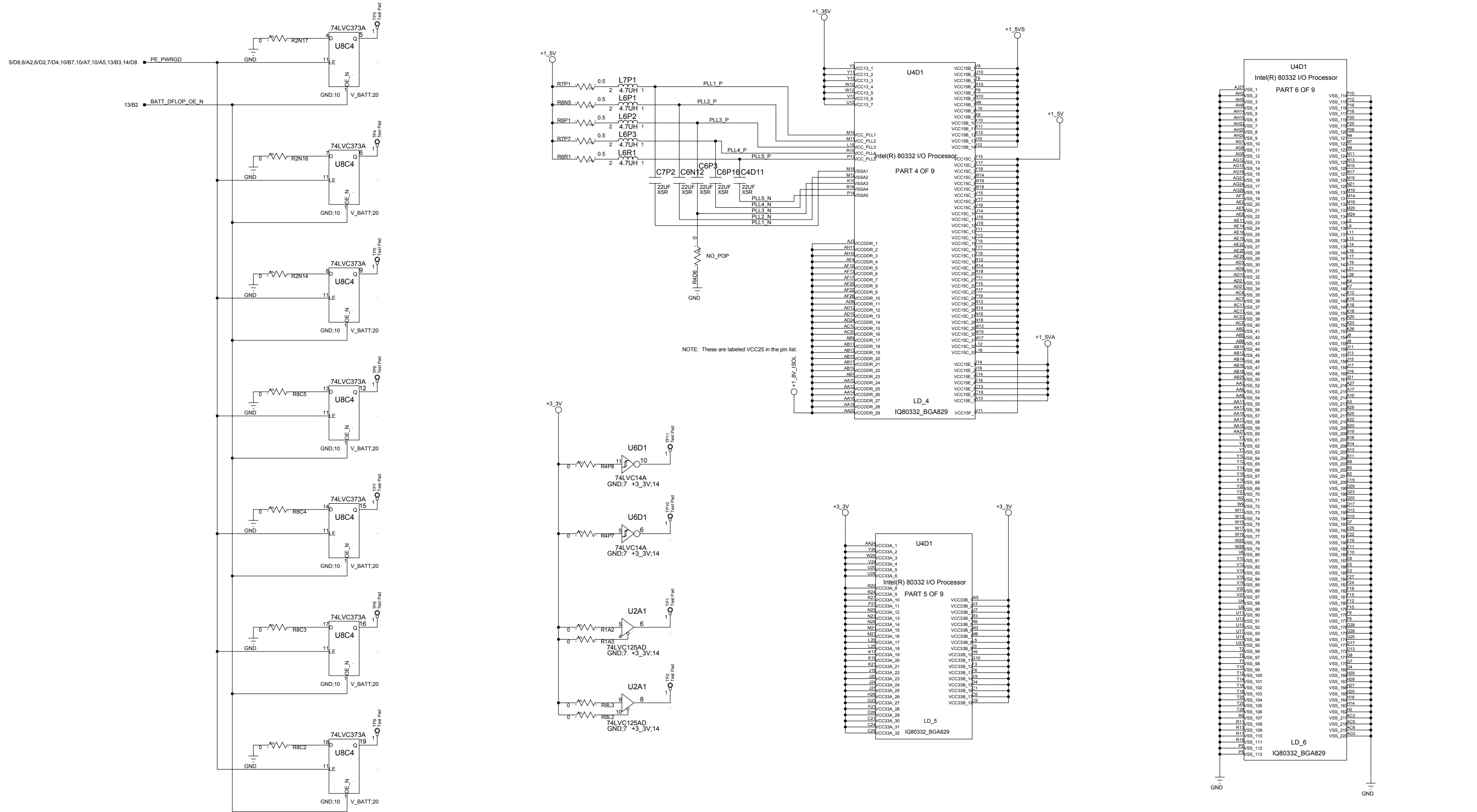
IOP JTAG Connector

CPLD JTAG Connector





FILTERED PHASE LOCK-LOOP SUPPLY



NOTE: These are labeled VCC25 in the pin list.

VERSION

VER 1.0 - PILOT

09/28/2004

DESIGN ENGINEER:
SCD HARDWARE ENGINEERING

DESIGN NAME:
80332 DDR-II 400 CRB

SHEET TITLE:

IQ80332 REVISION LOG

DATE MODIFIED:
9-27-2004_10:54

VERSION:
P 1.0

SHEET 17 OF 17