

WAN/LAN Access Switch Example Design for the Intel® IXP1200 Network Processor

Product Highlights

- Demonstrates a WAN/LAN access switch solution based on the Intel® IXP1200 network processor and other components of the total development environment
- Supports software-based Segmentation and Reassembly (SAR) of Ethernet packets and ATM cells
- Includes software-based Cyclic Redundancy Checking CRC-32 for enhanced reliability
- TCP/IP subsystem based on Big-Endian Linux* release available from the Linux open source community
- ATM subsystem for Linux from Trillium Digital Systems* Inc.
- Microcode software subsystem from Microware Systems Corporation*
- Provides the basis for value-added designs with fast time-to-market
- **Important note:** The WAN LAN Access Switch Example Design is a demonstration of products available to customers today. It is not in itself a product available to customers.

Overview

The Intel® Internet Exchange Architecture (Intel® IXA) provides a framework for the design of powerful and flexible networking and communication products. The WAN/LAN Access Switch Example Design demonstrates the application of a variety of Intel® IXA building blocks in a practical design, including the IXP1200 network processor, the cornerstone of the Intel® IXA. Offering unmatched flexibility and programmable performance, the IXP1200 network processor family is the foundation for a total development environment that includes a complete set of hardware and software building blocks and comprehensive software development tools designed to shorten time-to-market in a wide range of networking applications.

Intel develops example designs that illustrate

the flexibility and capabilities of the IXP1200 network processor and its total development environment. One important application segment is network access switching equipment for internetworking between an Ethernet LAN and an ATM WAN.

The purpose of this example design is to illustrate how Intel® IXA building blocks may be used in the design of similar applications. In addition, the design demonstrates the functionality and performance of the IXP1200 network processor family. Specifically, the design shows how ATM-Ethernet internetworking is handled by the IXP1200 network processor within the Intel® IXDP1200 Advanced Development Platform. The TCP/IP and ATM stacks reside on the Intel® StrongARM* core of the IXP1200 network processor, and the switch contains software-based SAR and CRC functionality in the IXP1200 network processor microengines. The access switch design also includes a Linux application based on the Big-Endian Linux release available from the open source community. This example design represents one of several possible software architectures that enable the IXP1200 network processor to be used in an entry-level ATM-Ethernet switch.

Based on the IXDP1200 Advanced Development Platform

The WAN/LAN Access Switch Example Design is based on the Intel IXDP1200 Advanced Development Platform. The design utilizes the Intel® IXM1200 Network Processor Base Card and the optional Intel® IXD4521 WAN I/O Option Card. The base card is contained in a compact PCI chassis and utilizes an ATM option card. Ethernet packets flow into and out of the base card, while the ATM cells flow into and out of the WAN I/O option card. Both are received and processed in the IXP1200 network processor 32-bit RISC microengines with hardware multithread support.

Note on the Availability of Software Components

Some software components used in this example design are not available from the open source community. In order to duplicate this example design, customers will either need to create non-open source components or buy the components directly from Microware Systems Corporation. In addition, components obtained from the open source community will need further development in order to function in this design. Software components may be obtained from the following sources:

- The AAL-5 driver conforms to the standard Linux driver framework and is available as a sample driver on the Intel® IXA Software Developers Kit (SDK) v2.0.
- The 10/100 Ethernet driver was created by Microware Systems Corporation. It is not included in the code obtained from the open source community.
- The ATM subsystem includes a Linux version of the Trillium System Services Interface (SSI). Customers will need to purchase the ATM software modules from Trillium Digital Systems.

For additional details on the availability of software components, please refer to the application note: WAN/LAN Access Switch Example Design For the IXP1200 network processor available on the Intel® IXA Web site: www.intel.com/ixa.

Six WAN/LAN Access Switch Microengines

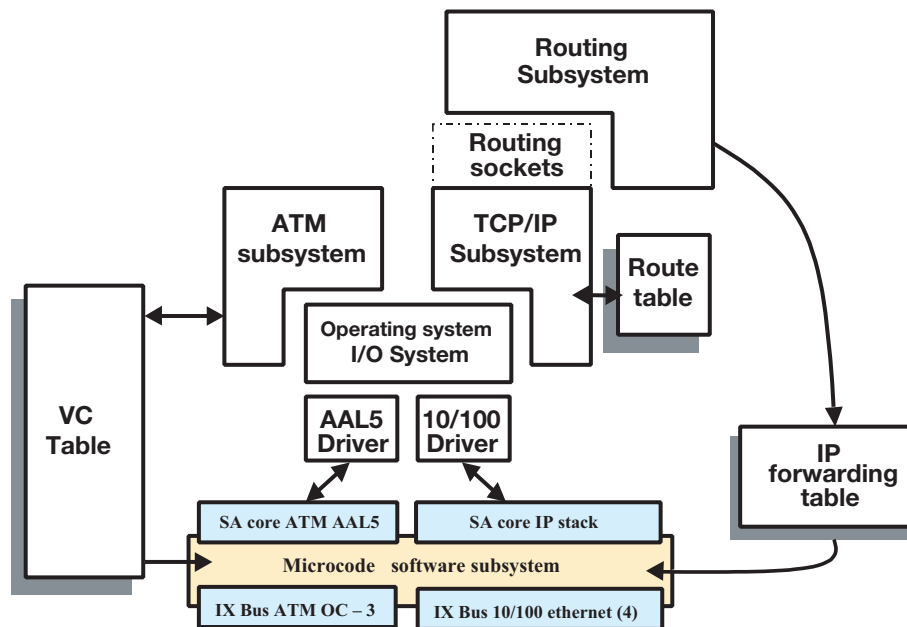
Six integrated programmable microengines run AAL-5 microcode, available from Microware* Inc., for the quick processing of ATM cells. The six microengines have code space for activities required by the switch. The Access Switch uses 4 of six microengines. Developers can use the remaining capacity to run custom code.

The microcode software subsystem includes execution threads for Ethernet receiver/IP forwarding, Ethernet transmitter, ATM receiver/forwarding, ATM transmitter, core AAL-5 service, core Ethernet service, and the AAL-5 CRC generator. The microengine subsystem feeds the packets/cells to the TCP/IP or ATM stack.

Microengine	Code Space Functions
Microengine 1	Four Ethernet Receive and Forward
Microengine 2	Four Ethernet Transmit and Forward
Microengine 3	Four empty code spaces
Microengine 4	One ATM OC3 Receive and Forward Two AAL5 CRC Receive One Intel® StrongARM* Core Ethernet
Microengine 5	One ATM OC3 Transmit Two AAL 5 CRC Transmit One Intel® StrongARM* Core AAL5
Microengine 6	Four empty code spaces

Features and Benefits

Feature	Benefit
Ethernet LAN - ATM WAN switch	Provides an example for the design of an entry level LAN/WAN switching devices
Supports OC-3 (155 Mbps) connection	Microcode that runs on Intel® IXP1200 network processor microengines, with additional performance headroom available for value-added functions from Microwares* Microcode Solutions Library (MSL) product.
Software-based Segmentation and Reassembly (SAR)	Reduces cost by eliminating the requirement for dedicated hardware SAR
Software-based Cyclic Redundancy Checking (CRC)	Enhances data integrity through error detection and correction
AAL-5 services	Supports quality connection-oriented variable-bit-rate (VBR) data traffic
Runs on Intel® IXDP1200 Advanced Development Platform	Demonstrates performance of the Intel® IXP1200 network processor and other components of the total development environment in LAN/WAN switch applications



Software Diagram of the WAN/LAN Access Switch Example Design on the Intel® StrongARM® Core

Modules & Software Components Supported

The following software components make up the Linux software subsystem for the WAN/LAN access switch example design:

AAL-5 Driver

The AAL-5 driver provides the interface between the ATM AAL-5 interface of the microcode software subsystem and the ATM subsystem interface. AAL-5 packets support quality connection-oriented variable bit rate non real time (VBR-nrt) data traffic and signaling messages. AAL-5 services are suitable for supporting internetworking between most data networking protocols.

10/100 Ethernet Driver

The 10/100 Ethernet driver provides the interface between the Ethernet interface of the microcode software subsystem and the TCP/IP subsystem.

Linux operating System & I/O

The Linux operating system and standard I/O system for Linux provides an open/close/read/write I/O interface. The Linux kernel provides memory management, cache, management, and MMU control for the system.

ATM Subsystem

The ATM subsystem is Linux version of the Trillium System Services Interface and includes the ATM Signaling Stack and Protocol Layers over ATM (PLOA) protocols.

VC Table Manager

The VC table manager manages the VC table used by the ATM microcode to process ATM cells.

TCP/IP Subsystem

The TCP/IP subsystem consists of TCP, UDP, IP, ARP cache management, and the net-link socket interface. The TCP/IP subsystem interfaces into the IP Demux driver for sending IP packet to the ATM stack.

Routing Subsystem

The routing subsystem consists of three processes - Open Shortest Path First (OSPF), Routing Internet Protocols (RIP) versions 1 & 2, and the Forwarding Table Manager (FTMS). The OSPF and RIP protocols interface to the system by the net-link socket interface of the TCP/IP subsystem.

IP Demux

The IP Demux accepts incoming packets from the PLOA and TCP/IP and routes the packets to the appropriate endpoints.

Total Development Environment

In addition to the WAN/LAN Access Switch Example Design, Intel® IXA building blocks include a comprehensive set of silicon, development tools and software:

- Intel® IXP1200 network processor family
- Intel® IXDP1200 Advanced Development Platform
- Intel® IXA SDK 2.0
- ATM/OC-3 to Fast Ethernet IP Router Example Design
- Windows NT* Integrated Development Environment (IDE) for embedded Linux

Next-generation network solutions require faster and more agile development than can be achieved with ASIC-based designs. IXP1200 network processor building blocks are designed to work together, providing the faster time-to-market development environment required for next generation Internet applications. In addition to its competitive advantage for equipment manufacturers, this comprehensive development environment reduces development costs for intelligent network products and while helping to reduce the total cost-of-ownership.

Intel® IXA

Intel® IXA is an end-to-end family of high-performance, flexible and scalable hardware and software development building blocks designed to meet the growing performance requirements of today's networks. Based on programmable silicon and software building blocks, Intel® IXA solutions enable faster development, more cost-effective deployment and future upgradability of network and communications systems.

Intel Access

Developer's Site	developer.intel.com
Intel® Internet Exchange Architecture Home Page	www.intel.com/ixa
Networking Components Home Page	developer.intel.com/design/network
Other Intel Support: Intel Literature Center	developer.intel.com/design/litcentr (800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
General Information Hotline	(800) 628-8686 or (916) 356-3104 5 a.m. to 5 p.m. PST

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