Intel® IXP2800 and IXP2850 Network Processors

B1 Stepping Qualification Report

September 2004

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Contents

1.0 Introduction 5
1.1 Purpose / Scope 5
1.2 Product Description 5
2.0 Quality Validation (QV) 8
3.0 High Voltage Life Test (HVLT) 8
4.0 Electrostatic Discharge (ESD) 9
4.1 Human Body Model (HBM) 9
4.2 Charged Device Model (CDM) 9
5.0 Latch-Up 10
6.0 Power-On Contention (POC) 10
7.0 Package-Related Stresses 10
7.1 Temperature Cycling 10
8.0 Bake 11

Tables

1 Product Variants 5
2 Product Characteristics 6
3 Qualification Results 7
4 Quality Validation Results 8
5 Qualification Criteria 8
6 Electrical Test Results at Each Read-Point 9

Revision History

Date	Revision	Description
September 2004	001	Initial Release
September 2004	002	Revised for web posting.

1.0 Introduction

1.1 Purpose / Scope

This is the Production Release Qualification (PRQ) level reliability report for the B Stepping of the IXP2800 and IXP2850 (Crypto Unit version) Network Processor in the FCBGA2.B package. This report covers development and qualification of this product for the commercial temperature application range in accordance with standard Intel® Corporation requirements and is consistent with the historical Production Qualification (PDQ) level of Intel products following a Standards-based product qualification.

1.2 Product Description

The Intel® IXP2800 Network Processor delivers programmable high-performance processing power with flexibility to address a wide variety of LAN, WAN, and Telecommunications applications. The Intel® IXP2800 Network Processor will deliver to customers the performance of ASIC hardware with the programmability of a microprocessor.

This network processor is a second-generation, highly integrated, hybrid data processor that provides high-performance parallel processing power and flexibility to a wide variety of OC-192 networking, communications, and data-intensive applications. The network processor is designed specifically as a data control element for applications that require access to a fast memory subsystem, a fast interface to I/O devices such as network MAC devices, and processing power to perform efficient manipulation on bits, bytes, words, and double-word (Dword) data.

The Intel® IXP2800 Network Processor combines the state-of-the-art Intel XScale® core microprocessor with 16 independent 32-bit RISC data engines with hardware multi-thread support that, when combined, provide a total of 25.2 giga-operations per second. The Microengines contain the processing power to perform tasks typically reserved for high speed ASICs.

Table 1 describes the product variants.

Table 1. Product Variants

Version	Ambient Range	MM#	Frequency	Maximum Power	V_{CC} Core
RPIXP2800BA	0 – 70° C	862117	1.0 GHz	23 W	1.3 V ± 5%
RPIXP2800BB	0 – 70° C	855650	1.4 GHz	31.5 W	1.3 V ± 5%
RPIXP2850BA (Crypto Unit version)	0 – 70° C	862113	1.0 GHz	25 W	1.3 V ± 5%
RPIXP2850BB (Crypto Unit version)	0 – 70° C	862114	1.4 GHz	34 W	1.3 V ± 5%

Table 2 describes the product characteristics.

Table 2. Product Characteristics

Supply Voltages	3.3 V ± 5%: PCI, GPIO, SP, JTAG 2.5 V ± 5%: SPI-4 1.5 V ± 100 mV: QDR SRAM 1.3 V ± 5%: Core, PLL, DLL, RDR, Fuse
Silicon Process & Site	P861.0 and D2
Die Size	1.433 cm x 1.909 cm
Number of Transistors	82 million
Ta (operating)	0 to 70º C (commercial temperature range)
Maximum Tj	120º C
Assembly Site	Cavite, Philippines
Test Site	Massachusetts Validation Center (MVC)
Package	1356 ball FCBGA2.B, 37.5mm x 37.5mm with IHS 12 layers stack-up, 1.00mm solder ball pitch Substrate thickness 1.35 mm ± 0.125 mm
Production Tester	Schlumberger* GX (Sort) Schlumberger* IX (Class) Agilent* (Class)

Table 3 describes the qualification results for the Intel® IXP2800 and IXP2850 Network Processors.

Table 3. Qualification Results

Qualification Stresses	Qualification Criteria	Results
Electrical 3–Temperature Quality Validation	0 fail – 568 units from 3 lots, tested without guardbands at 105º C, 25º C, and 0º C after passing Production test: 500 DPM	0 fail – 568 units from 7 lots: Passed 500 DPM
High Voltage Life Test (HVLT): IMC (0 – 30 days) Early Life (1st year) Long Life (15 years) Predictability	400 units from 3 lots through 3, 48, 168, and 500 hours at burn-in conditions of 1.66 V core, 3.5 V I/O, and 120º C junction temperature: 500 DPM 200 FIT 100 FIT Predictable to process baseline	777 units from 7 lots through 3 hours, 565 units from 7 lots through 48 hours, 494 units from 7 lots through 168 hours, 459 units from 7 lots through 500 hours: Passed 500 DPM Passed 200 FIT Passed 100 FIT Passed Predictability
Electrostatic Discharge: Human Body Model (socketed) Charged Device Model (socketed)	0 fail – 4 units from 2 lots: 1000 V 0 fail – 9 units from 3 lots: 500 V	0 fail – 9 units from 3 lots: Passed 2000 V 0 fail – 12 units from 6 lots: Passed 500 V
Latch-up V_{cc} I/O	0 fail – 4 units from 2 lots: Burn-In Vcc +20%, 125° C Ipin = +/-100 mA, 125° C	0 fail – 4 units from 2 lots: Passed Vcc Latch up Passed I/O Latch up
Power On Contention	0 fail – 15 units from 3 lots: Burn-In Vcc, 6 hours, clock/reset disabled	0 fail – 15 units from 3 lots: Passed Power On Contention
Component Level Temperature Cycling (Condition B after IPC4 preconditioning)	0 fail – 36 units from 1 lot: 1000 cycles	0 fail – 224 units from 6 lots: Passed 1000 cycles
Component Level Bake (165° C)	0 fail – 100 units from 2 lots: 100 hours	0 fail – 100 units from 2 lots: Passed 1000 hours

2.0 Quality Validation (QV)

Quality Validation is performed after the production flow to verify Production test/QA Test guardbands, temperature range, mixing/process issues and test repeatability.

After standard production electrical test is performed (guardbanded program, production test temperature) at hot and cold production test conditions, units are re-tested at three temperatures using the QA program (un-guardbanded). Qualification criteria for QV is 500 DPM. Quality validation results are shown in Table 4.

Table 4. Quality Validation Results

Test	Number of Units	Number of Lots	Number of Failures
Class 110C then Class -5C	568	7	N/A
QA 105C	568	7	0
QA 25C	568	7	0
QA 0C	565	7	0

Result: IXP2800 and IXP2850 meet QV qualification criteria

3.0 High Voltage Life Test (HVLT)

High Voltage Life Test (HVLT) is used to characterize product early and steady-state fallout and to determine production burn-in duration required to meet reliability specifications. Qualification criteria for this product are described in Table 5.

Table 5. Qualification Criteria

Parameter	Purpose	Qualification Criteria	Results
IMC (1st 30 days)	Infant Mortality Control is a measure of control for silicon manufacturing process related defects.	500 DPM	500 DPM
Early Life (1st year)	Early Life is a measure of product fallout in the first year of use and reflects steady-state reliability.	200 FIT	200 FIT
Long Life (15 years)	Long Life is a measure of product fallout in the first year to 15 years of use.	100 FIT	100 FIT

Stress conditions were V_{cc} I/O 3.5 V, V_{cc} core 1.66 V, Tj of 120º C. Devices were electrically tested at each read-point. The test results are shown in Table 6:

Table 6. Electrical Test Results at Each Read-Point

Number of Units	Number of Lots	Cumulative Hours
777	7	3
565	7	48
494	7	168
459	7	500

Results of stress testing indicate that this product falls within predictable levels for qualification criteria noted above.

Result: IXP2800 and IXP2850 meet HVLT qualification criteria.

4.0 Electrostatic Discharge (ESD)

Electrostatic discharge (ESD) stress testing is conducted to measure device robustness to damage caused by ESD due to human handling (HBM), or device charging during the manufacturing and test process (CDM).

4.1 Human Body Model (HBM)

HBM MIL STD 883E Method 3015.7 Notice 8 was performed on a 512-pin Key Tek Zap Master tester. Qualification criteria for HBM ESD is 1000 V. Test results are shown below:

Stress Level	Number of Lots	Number of Units	Number of Failures
± 2000 V	3	9	0

Result: IXP2800 and IXP2850 meet HBM ESD qualification criteria.

4.2 Charged Device Model (CDM)

Socketed CDM ESD testing was performed on a 512-pin Key Tek Zap Master tester. Qualification criteria for CDM ESD is 500 V. Test results are shown below:

Stress Level	Number of Lots	Number of Units	Number of Failures
± 500 V	6	12	0

Result: IXP2800 and IXP2850 meet CDM ESD qualification criteria.

5.0 Latch-Up

Latch-up testing is performed to assure a product does not enter a latch up state when exposed to over/under-voltage conditions on supply pins or over/under-current on signal pins.

Latch-up testing was performed according to the test methodology established in JEDEC 17 using an RCOMP and high-z JTAG patterns to tri-state most pins. Latch-up trigger voltage was limited to +6V/-3V so as not to induce electrical overstress.

The product requirements for Latch-up are burn-in Vcc + 20% (power supplies) and +/- 100 mA (signal pins) at 125° C. Test results are shown below:

Stress	Number of Lots	Number of Units	Number of Failures
V_{CC}	2	4	0
I/O	2	4	0

Result: IXP2800 and IXP2850 meet Latch-Up qualification criteria.

6.0 Power-On Contention (POC)

POC is a condition in which unintentional high current paths are created between Vdd and Vss during situations when a CLK and/or reset signal is not present. POC failure can contribute to problems with burn-in and test and increases in customer issues. Electrical test was performed before and after 6 hours of burn-in at Production burn-in conditions with clock signal and reset disabled. All measured parameters were within expected limits. No power on contention failures were observed. Test results are shown below:

Stress	Number of Lots	Number of Units	Number of Failures
6-hour burn-in, clock/reset disabled	3	15	0

7.0 Package-Related Stresses

Temperature cycling and bake were performed at product level for the IXP2800 and IXP2850 Network Processors.

7.1 Temperature Cycling

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes, resulting in mechanical stresses that can manifest as package cracking or delamination, die cracking, bond integrity, or thin film cracking. Factors that may influence this failure mechanism are package type and mold compound, lead frame, fab process, die size, underfill and layout design. The temperature cycling test was designed to expose failures due to thermal cycling during device operation.

Prior to performing the Temperature Cycling test units are exposed to a preconditioning step which simulates the assembly process. Temperature Cycling is performed according to MIL-STD-883 Method 1010.5 Condition B (-55 – 125° C). Qualification criteria is 0 failures allowed out of 36 units from one lot stressed to 1000 cycles. At each readpoint, a number of units were pulled for CSAM delamination evaluation. No issues were seen in the CSAM units, and there were no electrical test failures. Test results are shown below:

Number of Units	Number of Lots	Cumulative Cycles	Number of Units Pulled for CSAM	Number of Failures
251	6	IPC4	15	0
220	6	250	17	0
20	1	300	1	0
194	6	350	16	0
205	6	550	17	0
171	6	750	16	0
137	6	1000	16	0

Result: IXP2800 and IXP2850 meet product-level Temperature Cycle requirements.

8.0 Bake

Bake stress is performed to expose high-temperature related failure mechanisms associated with the package bump interface. Qualification criteria is 0 failures out of 100 units from two lots stressed to 168 hours at 165° C Bake. Stress devices were taken from the previously qualified product stepping. Test results are shown below:

Number of Units	Number of Lots	Cumulative Hours	Number of Failures
100	2	48	0
100	2	168	0
100	2	500	0
98[1]	2	1000	0

1. Two units were mechanically damaged and pulled from stress.

Result: IXP2800 and IXP2850 meet product-level Bake requirements.