



Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processors: FAQs

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How do I obtain the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor datasheet, developer's manual, and programmer's guide?

The documents are available at:

<http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm>

Is there a design guide for using the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor?

Yes. The *Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Processors Hardware Design Guidelines* and *Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Processors Design Checklist* are available at:

<http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm#guide>

Why do I need the Intel® IXP400 Software?

The IXP400 software provides the binary image of the NPE firmware and the operating-system-independent Intel XScale® core APIs to communicate to the NPEs.

How can I check the version number of my IXP400 Software?

The IXP400 Software source code contains a version number in `\ixp400_xscalesw\src\include\IxVersionId.h`. It is set by `#define IX_VERSION_ID`.

What type of programmability is there with the microengines?

The Intel® IXP4XX Product Line and IXC1100 Control Plane Processors do not contain microengines. The processors have Network Processor Engines (NPEs).

Can I program the NPEs?

No. Currently the NPEs are not independently programmable by end users. They are fixed-function-processing units for which Intel provides APIs. Additionally, NPE microcode images can be downloaded to the NPEs through the ixNpeDI API. These images are available in the Intel® IXP400 Software, which is available at:

<http://www.intel.com/design/network/products/npfamily/ixp425swr1.htm>

The APIs are documented in the *Intel® IXP400 Software Programmer's Guide*.

Do the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processors NPEs support little-endian or big-endian mode or both?

The Intel XScale core of the processors can transfer data in either little or big endian mode. Its endianness is defined by the status of bit 7 of coprocessor 15. IXP400 Software Release 1.3 and later allows support of both little and big endian. For more information see the *Intel® IXP4XX Product Line of Network Processors and IXC1100 Control : Understanding Big and Little Endian Modes Application Note*, available at:

<http://www.intel.com/design/network/applnots/254237.htm>

Is there a development platform for the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor?

Yes, there is a common development platform for the processors. The Intel® IXDP425 / IXCDP1100 Development Platform can be ordered by contacting your local Intel sales representative. The MM# is 855572. Information on the platform is available at:

<http://www.intel.com/design/network/products/nfamily/ixdp425.htm>

Can the Intel® IXP400 Software be used with the original Intel® IXCDP1100 Development Platform?

Yes. IXP400 Software Release 1.2.1 and later can be used with the original IXCDP1100 Development Platform.

How can you boot the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor?

You can only boot the processors via flash on Chip Select 0.

What is the “AHB” in the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor?

The AHB is the advanced, high-performance bus. It is a 32-bit, 133-MHz AMBA-standard bus technology that supports burst transfers, split-transactions pipeline operations and multiple masters. The AHB allows data transfers between its masters and the SDRAM controller. For more information, refer to the *Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual*.

Do the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor support synchronous flash devices such as the Intel® K3 StrataFlash?

Yes, the processors can interface and work with synchronous flash such as the Intel® K3 StrataFlash. However, the processors do *not* support burst mode.

Can a PCI device — connected to the PCI controller of the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor — access SDRAM devices connected to the SDRAM controller?

Yes. The PCI controller can transfer data via the AHB bus to and from a SDRAM device connected to the SDRAM controller.

Is it possible to have an external DMA engine transfer data from the expansion bus to an external SDRAM device connected to the SDRAM controller?

No. An external DMA engine cannot master the expansion bus. However, IXP400 Software Release 1.1 and later versions allow the use of one of the NPEs as a DMA engine for DMA transfers to and from a device on the expansion bus.

What are the conditions of using the DMA access-layer code component?

The DMA access-layer component requires autonomous access to the NPE.

Can the DMA access layer pull Ethernet frames directly from an Ethernet NPE?

No. The DMA access layer is meant to offload the Intel XScale core from the task of moving data from a non-NPE-based peripheral to another non-NPE-based peripheral (including SDRAM). The ixEthAcc component of the IXP400 software is, in essence, an Ethernet DMA engine as it pulls in Ethernet frames and places them in SDRAM without the intervention of the Intel XScale core.

Can I put the DMA access layer on two NPEs at the same time?

No. The DMA access layer can only be put on one NPE. That NPE then behaves as a DMA engine.

How many ATM PHYs do the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor support?

The IXP400 software supports a maximum of 12 PHYs. The mini-DSLAM software supports a maximum of 24 PHYs.

How many simultaneous channels does a high-speed serial (HSS) port support?

The IXP4XX product line of network processors has a maximum of two HSS ports. The ixHssAcc component (from the IXP400 software) is required to access, configure, and control the HDLC and HSS coprocessors of the HSS ports. Each of the HSS ports supports two types of services: packetized (HDLC) services and channelized services. The HSS channelized service supports a maximum of 32 channels. The 32 channels can be selected from any one of the 128 time slots spread across the HSS interface.

How many time slots does an HSS port support?

The HSS packetized services support TDM signals and up to four HDLC termination points per port — one per E1/T1 trunk. Each termination point supports up to 32 time slots. Consequently, the maximum supported time slots per HSS port is 128.

Can the WAN/voice NPE of the Intel® IXP425 and Intel® IXP421 Network Processors simultaneously use the two HSS ports and the UTOPIA port?

No. If a customer is using both HSS interfaces at the same time, they cannot use the UTOPIA interface. If *one* HSS interface is being used, however, the UTOPIA interface can be used simultaneously. Information on the interfaces is available in the *Intel® IXP4XX Product Line and IXC1100 Control Plane Processors Developer's Manual* and *Intel® IXP400 Software Programmer's Guide*.

Why does security (DES/3DES/AES) performance vary by application?

Ethernet NPE B hosts the security coprocessors. That same NPE also hosts the Ethernet coprocessor, which has the media independent interface (MII) functionality. Because security and MII share the same NPE, performance will vary — depending on MII usage. For example, routing a large number of small, 64-byte IP packets while simultaneously performing cryptographic processing will have some impact. Routing a smaller number of larger 1400-byte IP packets in the same situation will have a lesser impact.

How does the IXP400 Software Support Wireless Equivalent Privacy (WEP)?

The IxCryptoAcc API was enhanced in IXP400 Software Version 1.4 to include acceleration for the RC4 and CRC routines necessary for the 802.11i WEP specification. IxCryptoAcc supports

WEP in two ways; via an NPE-based engine on NPE-A, or an XScale core-based engine running on the XScale core. This is selectable when submitting the data to the API to be cryptographically processed.

The NPE-based WEP engine requires autonomous use of NPE-A. If NPE-A is needed for other purposes, the XScale core-based WEP engine should be chosen instead.

The Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor documentation says that the PCI controller and the expansion bus can run at a maximum of 66 MHz. How can I get the processors to generate a 66-MHz clock output?

The processors cannot generate a 66-MHz clock. The maximum speed of the internal clock generated by the processors is 33 MHz. GPIO 14 and GPIO 15 are the internal sources of this clock. To run the PCI controller or the expansion bus at 66 MHz, you'll need an external clock.

Can PCMCIA or a compact flash module directly interface with the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor?

Yes, a 16-bit PC card (PCMCIA, Compact Flash) connection can be done through the expansion bus, which has a 16-bit data bus. The customer has to develop the driver to support this device. For some additional information on a connection to Compact Flash, see the *Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processors : Expansion Bus Interface to Compact Flash Application Note*, available at:

<http://www.intel.com/design/network/applnots/254240.htm>

What is the function of the Queue Manager in the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor? How can it be managed?

The Queue Manager (QM) provides queuing functionality to the processors. Its primary role is to facilitate data flow from the NPEs to/from the Intel XScale core by passing 32-bit pointers to data structures that require processing and reside in SDRAM. It maintains 64 independent queues as circular buffers in an internal 8-Kbyte SRAM and implements the status flags and pointers required for each queue. The ixQmgr component of the IXP400 software allows configuration and control of the QM. That access layer also defines what queues are dedicated to the NPEs or to the Intel XScale core.

Does the Expansion bus support 32-bit, read-and-write accesses?

The expansion bus has a 16-bit physical interface that internally supports 32-bit reads, however 32-bit writes are *not* supported. Only 8- and 16-bit writes can be performed.

What is the maximum data frame size handled by the Intel® IXP4XX Product Line of Network Processors and IXC1100 Control Plane Processor UTOPIA, HSS, and Ethernet interfaces?

Each interface supports different data frame sizes.

- ATM-AAL 5

This interface can support PDUs up to 65,535 bytes or up to 256 chained mBufs, whichever is smaller. The PDU includes any padding needed to align on a 48-byte boundary and any AAL-5 trailer data.

- Ethernet

In the IXP400 Software Release 1.4, IxEthAcc can be configured to support Ethernet Frames up to 16,320 bytes.

- HSS-HDLC

The maximum recommended size for HDLC packets is 16 Kbytes. The HSS service can be configured to support up to 1024 bytes per frame for both transmit and receive.

How do I remove the PCI Support from the Linux* Kernel Intel® IXP400 Software's Linux* Support Package (LSP)?

To remove the PCI component from the Linux Kernel LSP:

1. Modify the file `arch/arm/config.in` by doing the following:

Change the line

```
define_bool CONFIG_PCI y
```

to

```
define_bool CONFIG_PCI n
```

2. Run `make menuconfig` and save.

This will update the top-level `.config` file.

3. Modify the file `arch/arm/mach-ixp425/Makefile` by removing all the `.o` file names that have `pci` in the name, so the Makefile looks like the following:

```
obj-$(CONFIG_ARCH_IXP425) += ixp425-irq.o ixp425-gpio.o ixp425-io.o
```

```
obj-$(CONFIG_ARCH_IXDP425) +=
```

4. Modify the file `arch/arm/mach-ixp425/ixp425-io.c` by changing the reference of the following functions to a NULL function:

- `outb`
- `outw`
- `outl`
- `inb`
- `inw`
- `inl`

How long — after `PWRON_RESET_N` goes to logic 1 — does the boot access start?

The access of the boot device starts when `RESET_IN_N` goes to logic 1 and `PLL_LOCK` goes to logic 1. A minimum of 10 ns is needed to hold `RESET_IN_N` at state 0 before it goes to state 1 and a maximum of 10 μ s is needed before `PLL_LOCK` changes state to 1. After these delays the first instruction of the boot access will start.

The processor boots up intermittently, what is a common cause of this?

If you are using the JTAG interface, you must pull `JTAG_TRST_N` high with a 10-K Ω resistor. If the interface is unused, you must pull `JTAG_TRST_N` low with a 10-K Ω resistor. Failure to do so may result in the processor booting intermittently.



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