

Intel® PXA255 Processor based Portable Media Player Reference Design Specification

Extended Computing Division (XCD)

Intel® Corporation

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1.0 Introduction

1.1 Overview:

Intel's Portable Media Player Reference Design is based on the Intel® PXA255 Applications Processor. The intent of this Reference Design is to quickly enable OEM's and ODM's developing Portable Media Players by providing a hardware design that offers many of the features for a Portable Media Player Design.

1.2 Development Goals:

- Deliver a platform designed specifically for Portable Media Players using application processors based on the Intel® XScale core. This particular spec defines the reference platform PCBA and associated peripherals to develop a Portable Media Player system.
- Enable software development.

1.3 Platform Overview

1.3.1 Main Board

The Main board contains:

- Intel® PXA255 Applications Processor, an Intel® XScale core based CPU, running up to 400MHz.
- 32MB of Intel® Strata-Flash™ memory or 2MB of Intel® Boot Block Flash
- 64MB of SDRAM at 100MHz
- LCD display
- Backlight for display
- Stylus/Touch Screen Input
- 13 HW Buttons (SW controlled)
- Brightness, Volume and UI
- Client USB 2.0 device port
- NTSC or PAL TV out (external)
- LION Battery and external DC power connector
- Speaker
- Head Phone connector

1.3.2 Daughter board

The Daughter board connects to the main board with a 100 pin connector and contains the following.

- Compact Flash connector for inserting a Compact Flash card.
- Right angle ATA connector for attaching the 2.5" 30Gig Hard Drive
- CPLD for creating the ATA decode signals.

1.4 Technical Features Overview

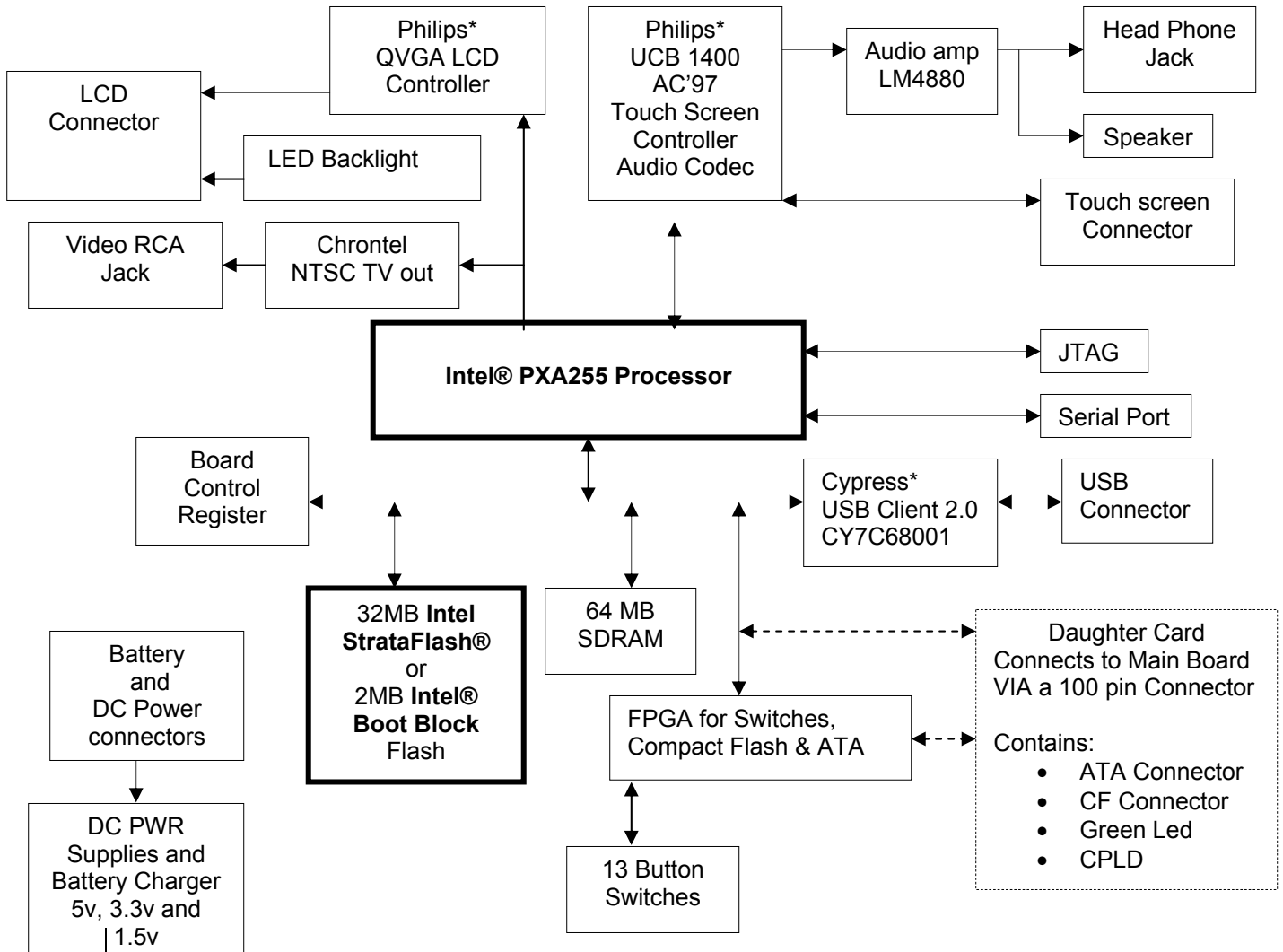
Table 1 5 Development Platform Feature List table

Feature	Interface	Description
Intel® PXA255 Processor 400 MHz	32 bit data bus	
64 MB SDRAM	Intel® PXA255 Processor(32 bit)	100 MHz
2 or 32 MB Intel® Flash Memory	Intel® PXA255 Processor (16 bit)	Supports 3V Advanced Boot Block or 3V Intel StrataFlash®
Philips* Embedded Display Controller	Intel® PXA255 Processor (32 bit bus)	<ul style="list-style-type: none"> ○ 50 MHz data bus ○ 2D/2.5D Engine
Philips* LCD Display	Intel® PXA255 Processor	<ul style="list-style-type: none"> ○ 320 x 240 resolution ○ 3.8" Diagonal ○ Touch Panel
Touch Screen	Screen (UCB 1400)	<ul style="list-style-type: none"> ○ 12 bps @ 100 samples/sec ○ 4 wire resistive
Cypress* USB Client Port	Intel® PXA255 Processor client USB device port	
Chrontel* NTSC\PAL TV out	CH013B	○ TV out Encoder
Audio	Intel® PXA255 Processor AC'97 link to Philips* UCB1400	○ Head Phone Output
Internal Stereo Speaker	Audio Amplifier	4 Ohm, 1 watt, circular speaker
13 HW Buttons	CPLD	Software Controlled
Soft system reset	Intel® PXA255 Processor reset input	3.3V not in regulation and momentary contact switch.
On/Off Switch	GPIO 0	Software controlled On/Off momentary contact button.
12V DC Input Power	2.5mm internal diameter 5.5mm external power plug	Power Adapter
Battery Controller ()	Intel® PXA255 Processor	Integrated into the battery pack.
Li-Ion Battery	Panasonic	2000 mAh
RS232 DB9	Intel® PXA255 Processor FF UART	Serial debug port no flow control

1.5 System Block Diagram

Intel Portable Media Player Reference Design Block Diagram

For a more detailed block diagram please refer to Reference schematic (page 2)



2.0 Physical Description

2.1 System Memory Map

Shows the address ranges for the reference platform, including SDRAM, flash memory, peripherals, and the system control and debug registers.

Table 2 System Memory Map

Address Range	Resource Size	Function	Functional Space
0000 0000 - 03FF FFFF	CS0 - 64 MB	Flash Bank 0	0 – 1FF FFFF
0400 0000 - 07FF FFFF	CS1 - 64 MB		400 0000 --5FF FFFF 600 0000 – 7FF FFFF
0800 0000 - 0BFF FFFF	CS2 - 64 MB	BCR Register	800 0000 – 9FF FFFF A00 0000 – BFF FFFF
0C00 0000 - 0FFF FFFF	CS3 - 64 MB	Key-switch Data	C00 0000 – DFF FFFF E00 0000 – EFF FFFF
1000 0000 - 13FF FFFF	CS4 - 64 MB		1000 0000 – 13FF FFFF
1400 0000 - 17FF FFFF	CS5 - 64 MB		1400 0000 – 17FF FFFF
1800 0000 - 1BFF FFFF	64 MB	RESERVED	
1C00 0000 - 1FFF FFFF	64 MB	RESERVED	
2000 0000 - 2FFF FFFF	256 MB	RESERVED	
3000 0000 - 3FFF FFFF	256 MB	RESERVED	
4000 0000 - 43FF FFFF	64 MB	Memory-Mapped (MM) Registers (peripherals)	
4400 0000 - 47FF FFFF	64 MB	MM Registers (LCD)	
4800 0000 - 4BFF FFFF	64 MB	MM Registers (Memory Ctrl)	
4C00 0000 - 4FFF FFFF	64 MB	RESERVED	
5000 0000 - 5FFF FFFF	256 MB	RESERVED	
6000 0000 - 6FFF FFFF	256 MB	RESERVED	
7000 0000 - 7FFF FFFF	256 MB	RESERVED	

8000 0000 - 8FFF FFFF	256 MB	RESERVED	
9000 0000 - 9FFF FFFF	256 MB	RESERVED	
A000 0000 - A3FF FFFF	64 MB	SDRAM - partition 0	nSDCS_0, Up to 64MB
A400 0000 - A7FF FFFF	64 MB	RESERVED	
A800 0000 - ABFF FFFF	64 MB	RESERVED	
AC00 0000 - AFFF FFFF	64 MB	RESERVED	
B000 0000 - BFFF FFFF	256 MB	RESERVED	
C000 0000 - CFFF FFFF	256 MB	RESERVED	
D000 0000 - DFFF FFFF	256 MB	RESERVED	
E000 0000 - EFFF FFFF	256 MB	RESERVED	
F000 0000 - FFFF FFFF	256 MB	RESERVED	

3.0 Hardware Details

This section provides a detailed description of the hardware subsystems on the Intel Portable Media Player Reference Design.

3.1 Platform Components

The reference system consists of Mainboard and Daughter Card

3.1.1 Platform hardware components:

- Intel® PXA255 Processor
- Intel StrataFlash® or Boot Block Flash
- SDRAM
- Board Control Register (BCR)
- LCD Display Components
 - Display
 - Backlight
 - Grey-scale
 - Connector
- Touch Screen
- NTSC TV out Components
- Compact Flash Interface
- USB 2.0 Client Controller
- RS232 Serial port
- Audio
- Lion Battery and Charging
- ATA Interface with 2.5" 30G Hard Drive
- Daughter Card Address and Data Buffers
- CPLD on Main Board in support of CF and ATA HDD
- CPLD on Daughter Card for HDD Support
- DC to DC power supplies

3.2 Intel StrataFlash® or Boot Block Flash (Bottom Boot type) Interface

The reference design supports two – 64 ball Easy BGA footprints. One 3V Boot Block device supports 2MByte to 16MByte non-volatile memory size **or** One 3V Sync Intel StrataFlash® device supports 8MByte to 32MByte non-volatile memory size.

Both types may be not populated at the same time.

The ROM Memory is programmable via the Intel® PXA255 processor JTAG port for initial program load. The flash array is configured as 16-Data bits. All reads and writes are 16 bits. The Boot Select pins on the processor are configured to support these 16 bit ROM accesses. Typically the Boot Block Flashes will be the chosen component for platform because it is probable that 2 MB of flash will be sufficient.

3.3 SDRAM Interface

The Reference Design supports two SDRAM TSOP footprints for a 32 bit wide partition. This allows use of devices ranging from 8MBytes to 32MBytes. Two 32MByte devices are soldered directly onto the board providing 64Mbytes of memory. The board layout minimizes trace lengths

and parallelisms to provide support for a 104MHz data rate. The memory is connected for legacy SA1110 mode.

3.4 Board Control Register (BCR)

The BCR is a LVC16374 that is selected and set by the Intel® PXA255 processor. It is a register used for setting the functions in the following table.

Data is latched if NCS2 = 0 and New- = 0 and Not Reset = 1. Default = 0.

The circuit is:

Intel® PXA255 processor => LVC 16374 => Various output control destinations (see Table below for details.)

Bit 0	Reserved	Don't Care	
Bit 1	USB2_NRST	Active Low	USB 2.0 Reset
Bit 2	CF_RESET	Active High	Compact Flash Reset
Bit 3	Reserved	Don't Care	
Bit 4	ATA_RESET	Active High	Hard Drive Reset
Bit 5	Reserved	Don't Care	
Bit 6	Reserved	Don't Care	
Bit 7	BACKLIGHT_PWR_ON	Active High	Enable LCD Backlight Power
Bit 8	LCD_PWR_ON	Active High	Enable LCD Power
Bit 9	RS232_ON	Active High	Enable RS232
Bit 10	Reserved	Don't Care	
Bit 11	Reserved	Don't Care	
Bit 12	NGREEN_LED	Active Low	Turn on Green LED
Bit 13	Reserved	Don't Care	
Bit 14	Reserved	Don't Care	
Bit 15	Reserved	Don't Care	

3.5 LCD VIDEO

The LCD panel is a Philips* 3.8" QVGA transfective Active Matrix color LCD (AMLCD) module. The display resolution is 240 x RGB x 320 dot matrix pixels portrait QVGA, driven through an 18-bit interface that allows selection of 260k colors maximum.

The reference design LCD panel chain is:

Intel® PXA255 processor video out => Philips* LCD controller => Philips* TFT LCD display panel.

3.6 Touch Panel

The reference design contains a 4-wire resistive touch screen integrated onto the Philips LCD Panel.

The touch screen circuit is:

Philips* LCD panel => Touch screen connector => Philips* UCB1400 => Intel® PXA255 Processor.

The sensor connects to the 4 pin FPC connector using a 1.0 mm pitch ZIF flexible cable.

3.7 NTSC TV out

The reference design provides an NTSC output for connection to a NTSC or PAL television by connecting the Intel® PXA255 processor video output to a Chromtel* CH013B Encoder.

3.8 Compact Flash

The Compact Flash chain for the reference design is:

Intel® PXA255 Processor PCMCIA signals => XMR3032XL CPLD => STD. Compact Flash connector.

3.9 USB 2.0 Client

The reference design contains a Cypress* USB 2.0 client CY68001 to allow the board to communicate with a USB host. This port is primarily used for transfer of data between the reference design and the host computer.

3.10 RS232 Port FF UART

The reference design provides a “partial function” RS-232 interface. This is connected to the Intel® PXA255 processor’s full function UART via a RS-232 transceiver that resides on the main board. This serial communication port is designed to be used as a development debug interface or an applications communications interface. No hardware flow control is supported on this port.

3.11 Audio

The Philips* UCB1400 AC'97 Codec provides the following audio functions:

- Amplified headphone output for 32-ohm output load.
- 16-bit stereo full duplex CODEC

3.11.1 Headphone Output

The reference design provides a 3.5mm jack for 32K ohm headphones.

3.11.2 External Mono Speaker

The reference design provides one case mounted speaker. The external speaker is a circular 4 Ohm, 1 watt speaker.

3.11.3 Audio Power Amplifier

The reference design provides one LM4880 Audio Power Amplifier with a shutdown mode of operation. The Amplifier connection is:

Philips* UCB 1400 Line Out => LM4880 Amplifier => 2 pin connector => Case mount speaker

The speaker is designed to provide for a portable, low voltage application. When not in use, the CODEC automatically powers off the audio amplifier to further conserve power.

Note: Minimal power is supplied to the external speaker for this reference design and is intended solely for proof of design.

3.12 Battery

A battery is included in the reference design to provide mobile operation.

3.12.1 Lithium Ion Battery

The battery is a single module consisting of 2 serially connected Panasonic Lithium Ion batteries that provide 7.2 V at 2.0 Ah. The Module is a Micro Power Electronics* model MPE 888-555-002.

3.12.2 Charging

The batteries are recharged on the reference design with an “on board” MAX846 Battery Charger IC circuit when the device is powered with the wall mount 12v Power supply.

The charge level is monitored by the CPU with the following circuit.

Battery output => Philips* UCB1400 AD input => Philips* UCB1400 digital output => Intel® PXA255 Processor.

The charge level is reported to the Operating System in .1v increments. Maximum charge level occurs at approximately 8.1v and system shutdown occurs at approximately 5v.

3.13 ATA and CF Interface

3.13.1 Address and Data Buffers

One Address Buffer and 2 Data Buffers are included on the circuit board in order to isolate the Compact Flash and Hard Drive from the internal bus.

3.13.2 Daughter Card Connector

The daughter card connects to the Main Board via a 100 Pin connector. The daughter card contains the socket connectors for the both the Compact Flash card and the 2.5” Hard drive. Also, a Xilinx* CPLD is on board to support data and control signal multiplexing between the Hard drive and Compact Flash.

Table 3 Daughter Card Connector

PIN	SIGNAL	PIN	SIGNAL
1	3.3v	2	5v
3	GND	4	GND
5	CF_10	6	ATA_RESET
7	CF_9	8	ATA_7
9	CF_8	10	ATA_8
11	Reserved	12	ATA_6
13	Reserved	14	ATA_9
15	CF_nREQ	16	ATA_5
17	Reserved	18	ATA_10
19	CF_nWAIT	20	ATA_4
21	CF_RESET	22	ATA_11
23	Reserved	24	ATA_3
25	Reserved	26	ATA_12
27	3.3v	28	ATA_2
29	GND	30	ATA_13
31	CF_nREQ_IN	32	ATA_1
33	CF_nWE	34	ATA_14
35	CF_nIOW	36	ATA_0

37	CF_nIOR		38	ATA_15	
39	CF_VS1		40	5v	
41	CF_nCE2		42	GND	
43	CF_15		44	ATA_DMAREQ	
45	CF_14		46	ATA_nIOWR	
47	CF_13		48	ATA_nIOR	
49	CF_12		50	ATA_IORDY	
51	CF_11		52	ATA_DMACK	
53	CF_nC01		54	ATA_nREQ	
55	CF_nC02		56	ATA_nC01	
57	CF_nIOCS16		58	ATA_nC02	
59	3.3v		60	Reserved	
61	GND		62	Reserved	
63	CF_2		64	Reserved	
65	CF_1		66	CF_ATA_5	
67	CF_0		68	CF_ATA_4	
69	CF_ATA_0		70	CF_ATA_3	
71	CF_ATA_1		72	CF_ATA_2	
73	CF_ATA_6		74	5v	
75	CF_ATA_7		76	GND	
77	CF_ATA_8		78	ATA_nCE1	
79	CF_ATA_9		80	Reserved	
81	CF_nOE		82	Reserved	
83	CF_ATA_10		84	Reserved	
85	CF_nCE1		86	Reserved	
87	CF_7		88	Reserved	
89	CF_6		90	Reserved	
91	CF_5		92	Reserved	
93	CF_4		94	Reserved	
95	CF_3		96	Reserved	
97	3.3v		98	5v	
99	GND		100	GND	

4.0 Power System

The power system of the reference design has been designed with the following:

- DC Power Jack, (2.5/5.5mm) for external power source 12.0VDC minimum @ 2.0A
- 7.2 VDC, 2.0 Ah battery-pack for mobile operation.
- Provide a high-efficiency 3.3V supply rail for I/O and general system power
- Provide a high-efficiency 1.5V Core/PLL supply for the microprocessor
- Provide a high-efficiency 5.0V supply rail for PCMCIA and USB I/O and filtered power for the Audio System and LCD Analog supply.

4.1 Power System Configuration

No power switch is used to set the unit from a power off or power on state. A soft button (SW 13) is provided to put the system to sleep or low power state to or to wake the system up.

The 5V and 3.3 VDC are derived from the two synchronous step-down DC-to-DC Converters that are supplied by 12 VIN Power Brick or the battery.

Vcore is derived from the 5V rail via a high efficiency step-down low power DC-to-DC converter.

4.2 System Reset

A voltage monitoring supervisory circuit (MAX6816) is used to sense the 3.3V power supply rail and generate the reset signal to the processor nRESET input should the rail voltage drop below 3.08 V. A manual reset button (SW 12) is provided to force a system reboot on GPIO_0.

4.3 Wall mount power supply detect

A circuit that detects if the Wall Mount power supply is connected and powered reports status to the CPU.

The circuit is:

12v power supply brick out => voltage divider 4v out => FET => Intel® PXA255 processor GPIO

5.0 Appendix

Appendix A – GPIO Usage

Table 3 Development Platform GPIO List

GPIO Descriptions					
LEGEND: IAL INPUT ACTIVE LOW IAH INPUT ACTIVE HIGH OAH OUTPUT ACTIVE HIGH OAL OUTPUT ACTIVE LOW OCLK OUTPUT CLOCK ICLK INPUT CLOCK IP INPUT PROGRAMMABLE IDAT INPUT SERIAL DATA ODAT OUTPUT SERIAL DATA NU SPARE GPIO					
PIN	PIN #	Alternate Function Name	Signal Name	TYPE	Signal Description
GPIO0	L10	N/A	SW_ONOFF_OUT	IAL	This is the active low ON/OFF tactile, momentary, switch.
GPIO1	L12	GP_RST	USB2_WAKEUP	IAL	This is the SW reset input to the Intel® PXA255 Processor
GPIO2	L13	N/A	CF_nIREQ	IAL	
GPIO3	K14	N/A	CF_CD	IAL	
GPIO4	J12	N/A	ATA_nIREQ	TBD	
GPIO5	J11	N/A	ATA_CD	IAH	
GPIO6	H14	MMCCLK		IAL	
GPIO7	G15	48MHZ_CLK	FLASH_nWP	OAH	
GPIO8	F14	MMCCS0		OAH	
GPIO9	F12	MMCCS1	USB2_nIRQ		
GPIO10	F7	RTCCLK	SW_nIRQ		
GPIO11	A7	3.6MHZ	AC97_nIRQ		
GPIO12	B6	32KHZ			

GPIO13	B5	MBGNT	USB2_FLAGC		
GPIO14	B4	MBREQ	USB2_RDY_IRQ		
GPIO15	T8	CS1_N			
GPIO16	E12	PWM0			
GPIO17	D12	PWM1	NVBATT_LOW_I RQ		
GPIO18	C1	RDY			
GPIO19	N14	DREQ[1]			
GPIO20	N12	DREQ[0]			
GPIO21	N15	N/A			
GPIO22	M12	N/A			
GPIO23	F9	SCLK			
GPIO24	E9	SFRM			
GPIO25	D9	TXD			
GPIO26	A9	RXD			
GPIO27	B9	EXTCLK			
GPIO28	C9	BITCLK			
GPIO29	E10	SDATA_IN0			
GPIO30	A10	SDATA_OUT			
GPIO31	E11	SYNC			
GPIO32	A16	SDATA_IN1			
	D10	ACRESET_N			
GPIO33	T13	CS5_N			
GPIO34	A13	FFRDY			
GPIO35	A14	FFCTS			
GPIO36	A12	FFDCD			
GPIO37	B11	FFDSR			
GPIO38	B10	FFRI			
GPIO39	E13	FFTXD			
GPIO40	F10	FFDTR			
GPIO41	F8	FRTS			
GPIO42	B13	BTRXD			
GPIO43	D13	BTTXD			
GPIO44	A15	BTCTS			
GPIO45	B14	BTRTS			
GPIO46	B15	IRRXD			

GPIO47	C15	IRTXD			
GPIO48	P13	POE_N			
GPIO49	T14	PWE_N			
GPIO50	T15	PIOR_N			
GPIO51	R15	PIOW_N			
GPIO52	P14	PCE1_N			
GPIO53	R16	PCE2_N			
GPIO54	P16	PSKTSEL_N			
GPIO55	M13	PREG_N			
GPIO56	N16	PWAIT_N			
GPIO57	M16	IOIS16_S			
GPIO58	E7	L_DD[0]			
GPIO59	D7	L_DD[1]			
GPIO60	C7	L_DD[2]			
GPIO61	B7	L_DD[03]			
GPIO62	E6	L_DD[4]			
GPIO63	D6	L_DD[5]			
GPIO64	E5	L_DD[6]			
GPIO65	A6	L_DD[7]			
GPIO66	C5	L_DD[8]			
GPIO67	A5	L_DD[9]			
GPIO68	D5	L_DD[10]			
GPIO69	A4	L_DD[11]			
GPIO70	A3	L_DD[12]			

GPIO71	A2	L_DD[13]			
GPIO72	C3	L_DD[14]			
GPIO73	B3	L_DD[15]			
GPIO74	E8	L_FCLK			
GPIO75	D8	L_LCLK			
GPIO76	B8	L_PCLK			
GPIO77	A8	L_BIAS			
GPIO78	P9	CS2_N			
GPIO79	T9	CS3_N			
GPIO80	R13	CS4_N			

Appendix B – Schematics

Please contact your local Intel representative to obtain current schematics.