



Intel® PXA255 Processor based Portable Media Player Reference Design

Schematic Diagram

August 2004

Order Number: 301265-001



REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
1.0	FAB A		/				

INTEL (R)

- [1] REF: _TABLE_OF_CONTENTS]
- [3] INTEL (R) PXA255 PROCESSOR 1 OF 2]
- [4] INTEL (R) PXA255 PROCESSOR 2 OF 2]
- [5] INTEL (R) FLASH AND 64 MB SDRAM]
- [6] BCR REGISTER AND ALTERA CPLD]
- [7] CF BUFFERS, ATA BUFFERS AND MAIN BOARD CONN]
- [8] DAUGHTER BOARD CONN, CF CONN, XILINX* CPLD AND HDD CONN]
- [9] LCD CONTROLLER, LCD CONN AND LCD PWR]
- [10] CHRONTEL* CH013B NTSC TV OUT ENCODER]
- [11] PHILIPS* UCB1400 AUDIO AND TOUCH SCREEN]
- [12] JTAG CONN, RS232 AND CYPRESS USB 2.0]
- [13] BATTERY CHARGER AND 5 VOLT POWER SUPPLY]
- [14] 3.3 VOLT AND 1.5 VOLT POWER SUPPLIES]
- [15] BUTTON SWITCHES AND BYPASS]
- [16-21] ALTERA* AND XILINX* SCHEMATIC BASED CODE]

PBA CXXXXXX-001
 FAB A
 REV 1.1
 SCHEMATIC UPDATED: 07/26/04

NOTES:

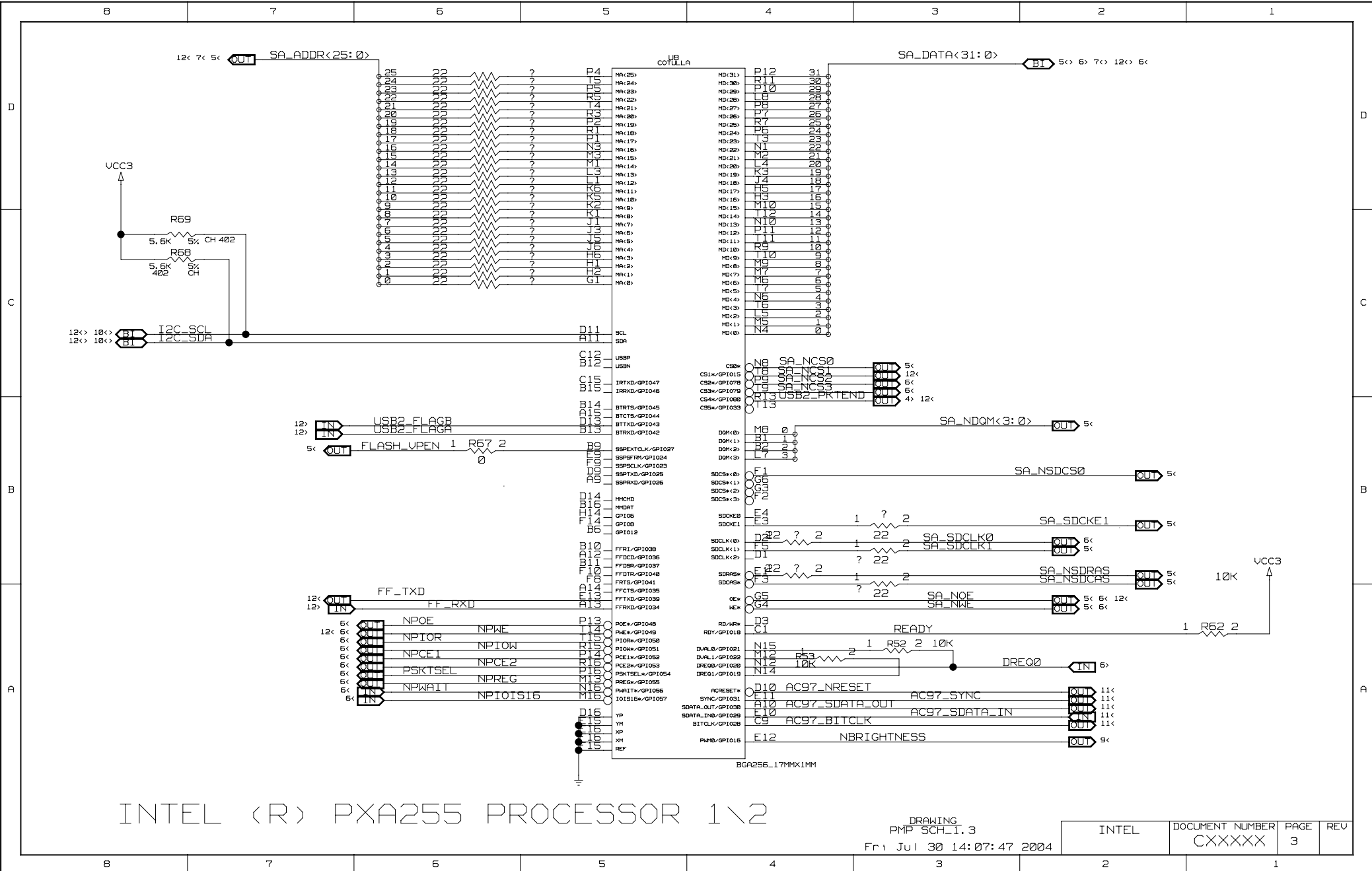
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLS FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

PORTABLE PERSONAL MEDIA PLAYER

* 3RD PARTY BRANDS AND NAMES ARE PROPERTIES OF THEIR RESPECTIVE OWNERS.

BOM RELEASE DATE	xx/xx/xx	PB NUMBER CXXXXX-001			
SIGNATURE	DATE	intel		3065 BOWERS AVE SANTA CLARA, CA 95051	
DRN BY					
CHK BY		TITLE SCH, PBA, PMP			
ENGR APVD					
APVD		INTEL	DOCUMENT NUMBER	PAGE	REV
APVD			CXXXXX	1/21	10

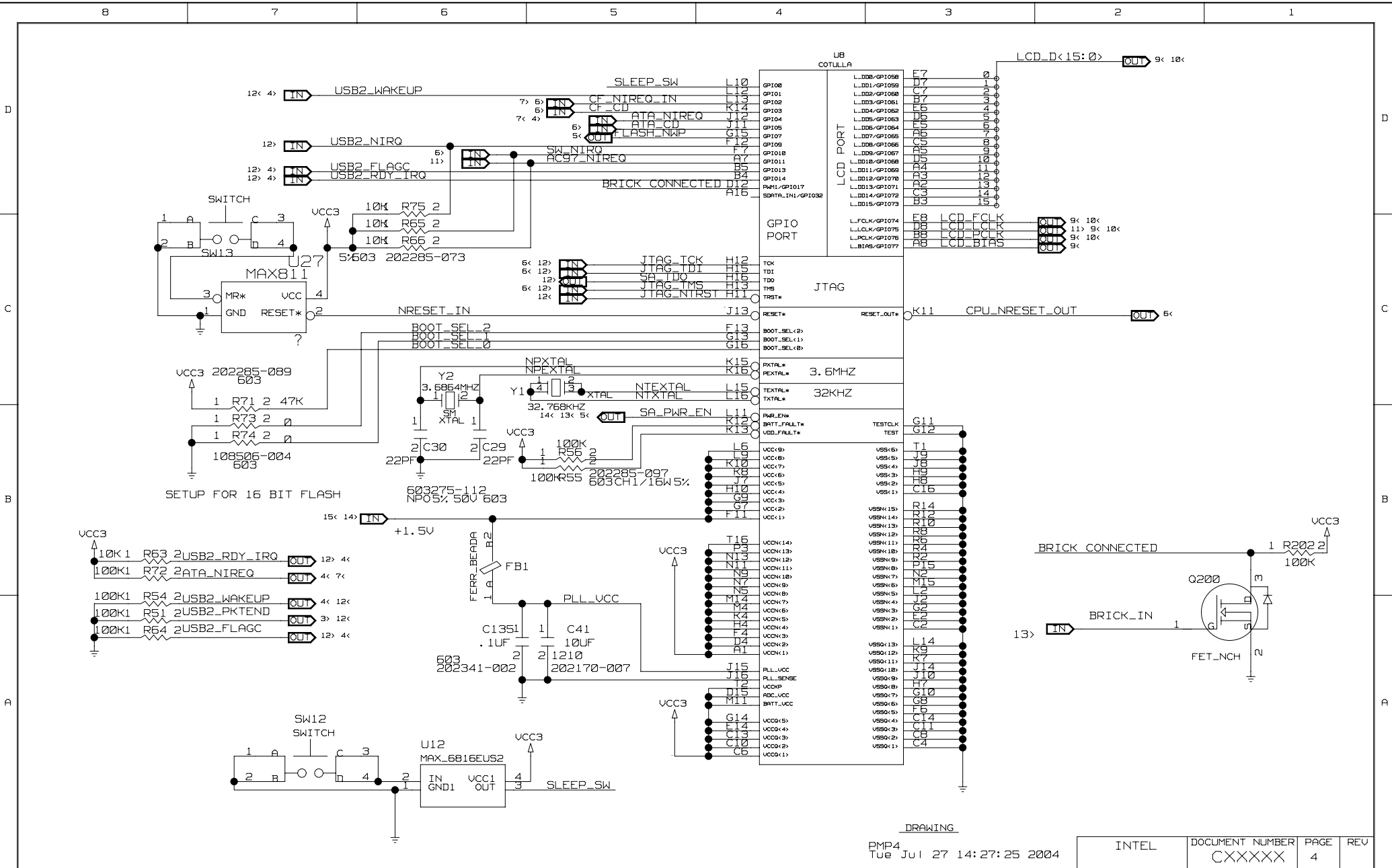
DRAWING
 PMP_SCH_1.1
 Wed Aug 04 13:58:46 2004



INTEL (R) PXA255 PROCESSOR 1\2

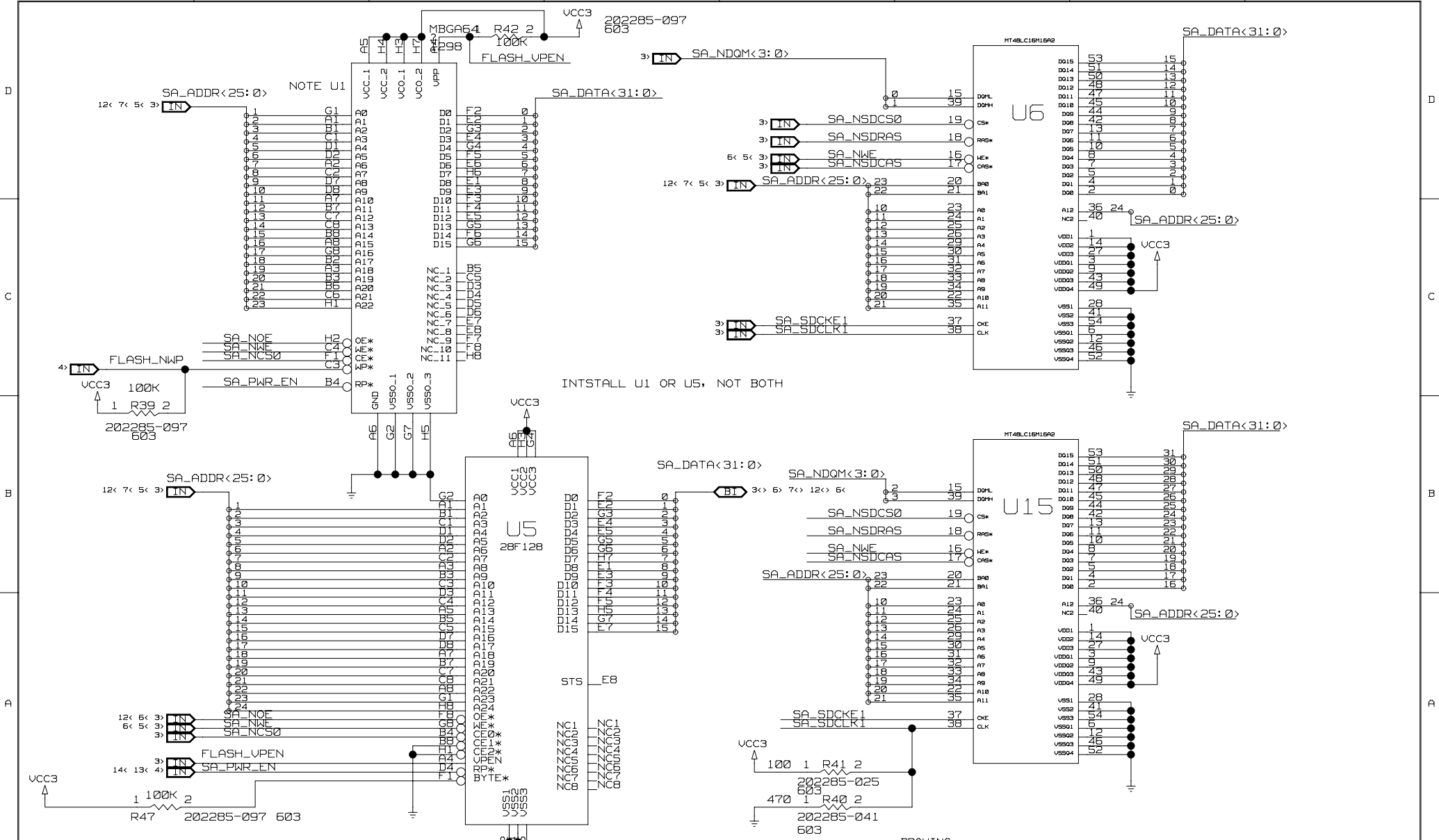
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PMP4
Tue Jul 27 14:27:25 2004

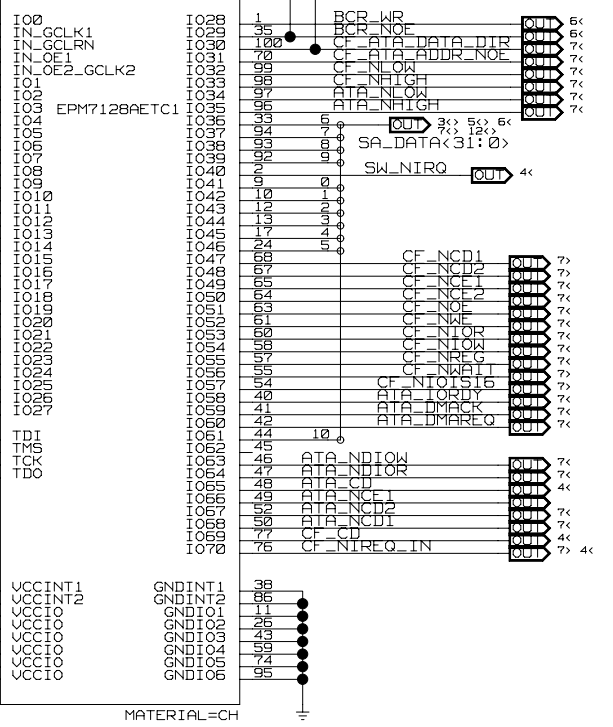
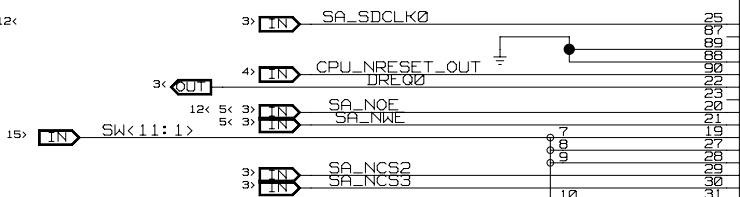
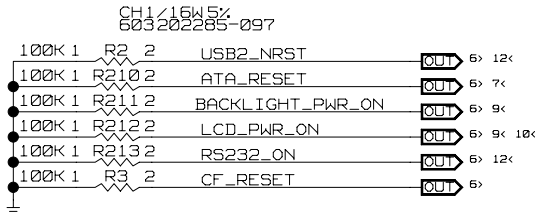
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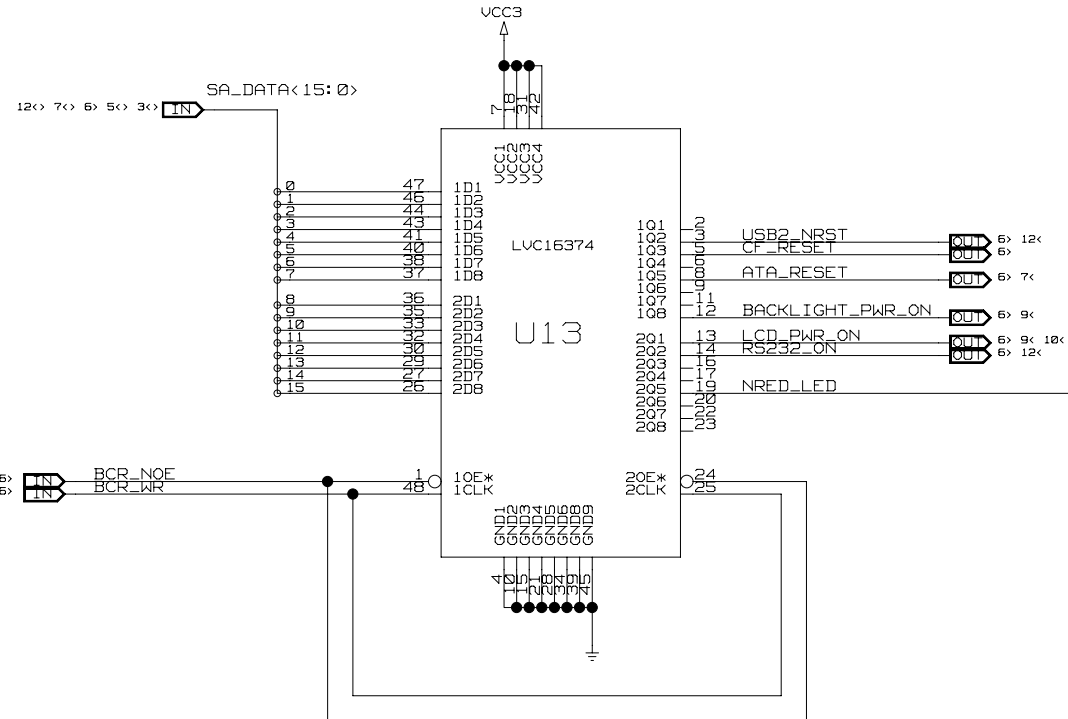
[PAGE_TITLE= FLASH AND SDRAM]

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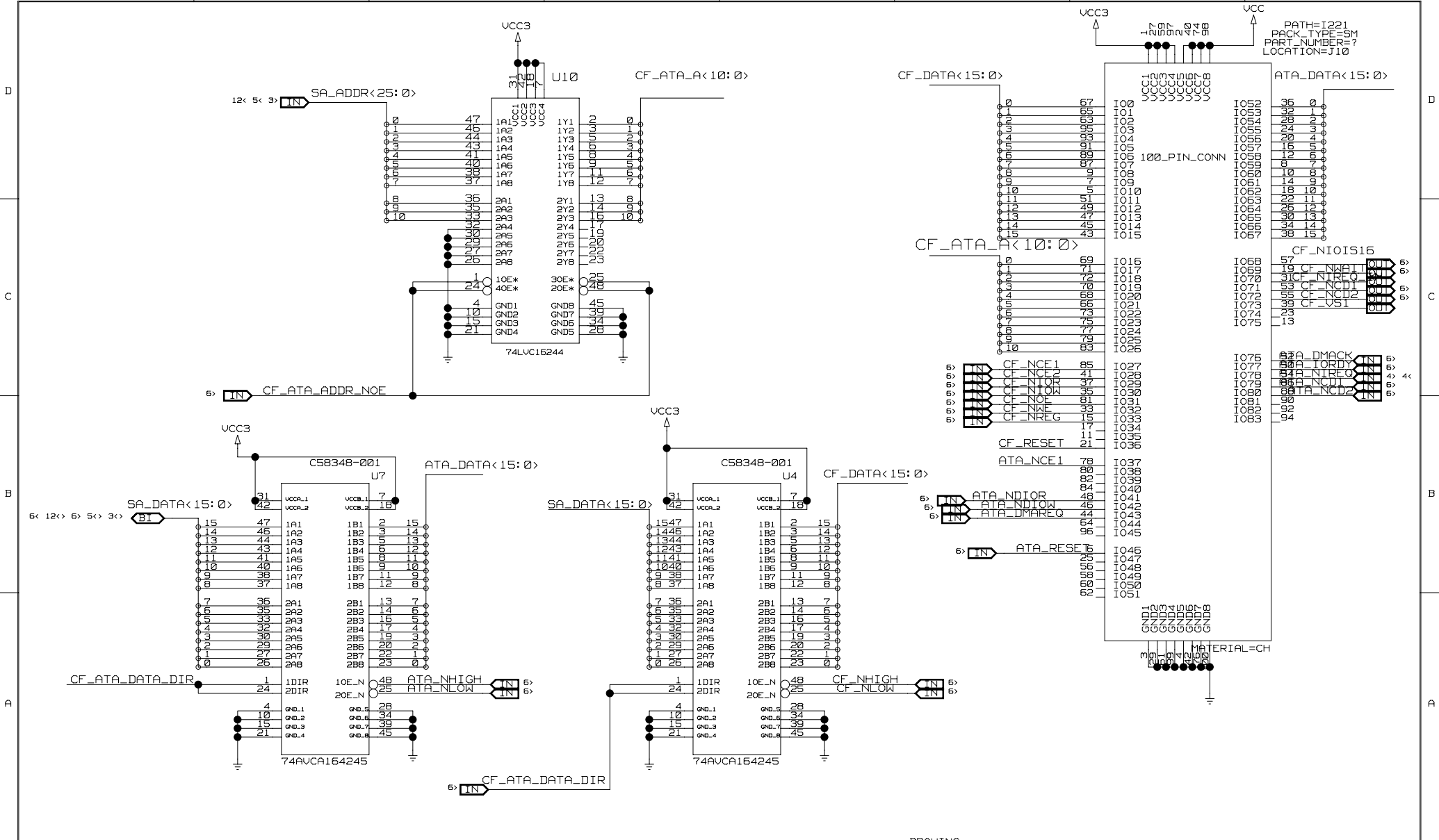
BCR REGISTER (BCR)



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PMP_SCH_1_6
Wed Jul 28 14:21:10 2004

[PAGE_TITLE= BCR, BUTTONS, FPGA]

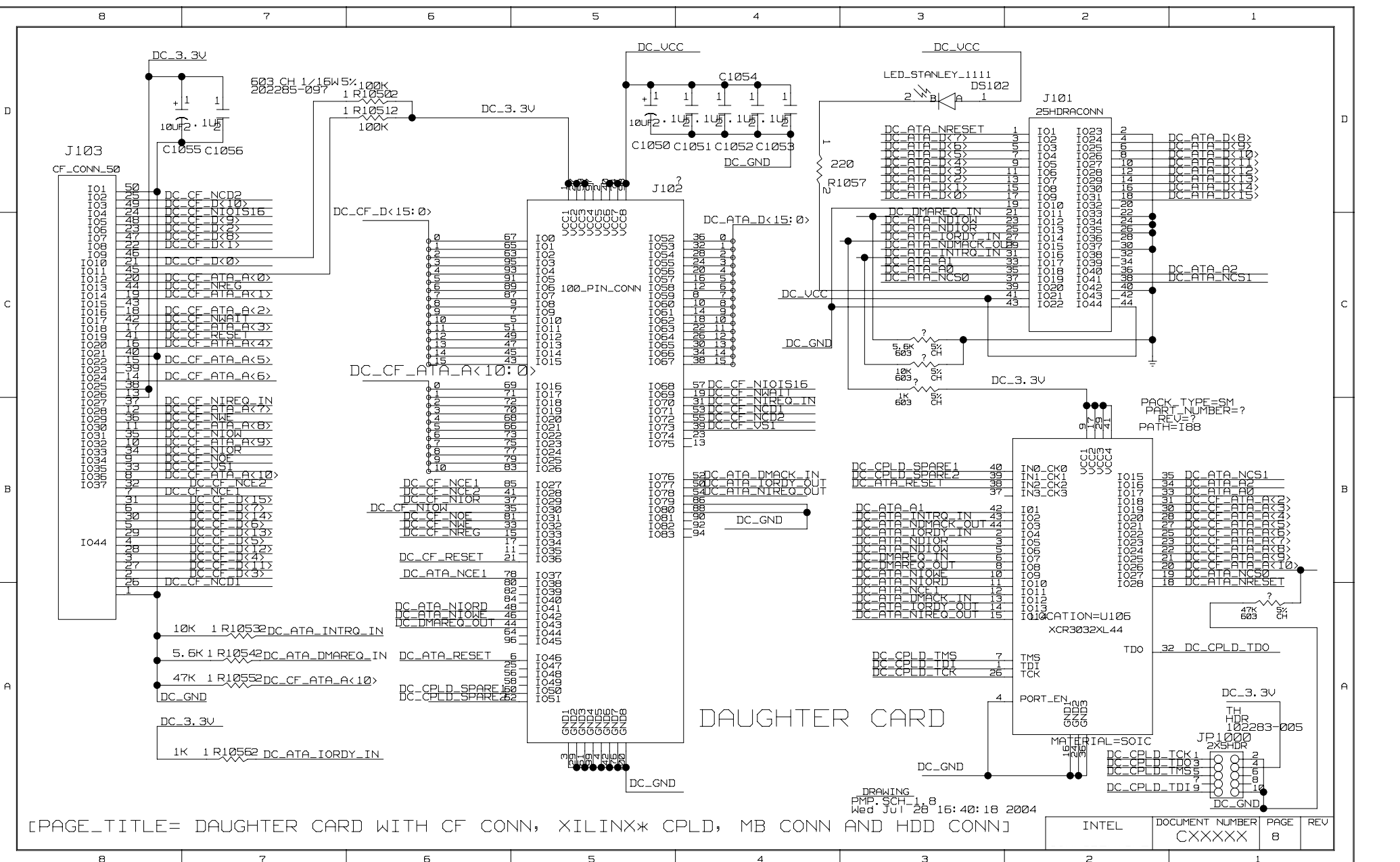
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[PAGE_TITLE= CF_LATA ADDRESS/DATA BUFFERS]

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Wed JUL 28 16:41:03 2004

INTEL	DOCUMENT NUMBER	PAGE	REV
	CXXXXX	7	



DAUGHTER CARD

DRAWING PMP_SCH_1_8 Wed Jul 28 16:40:18 2004

[PAGE_TITLE= DAUGHTER CARD WITH CF CONN, XILINX* CPLD, MB CONN AND HDD CONN]

INTEL	DOCUMENT NUMBER CXXXXX	PAGE 8	REV
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8

7

6

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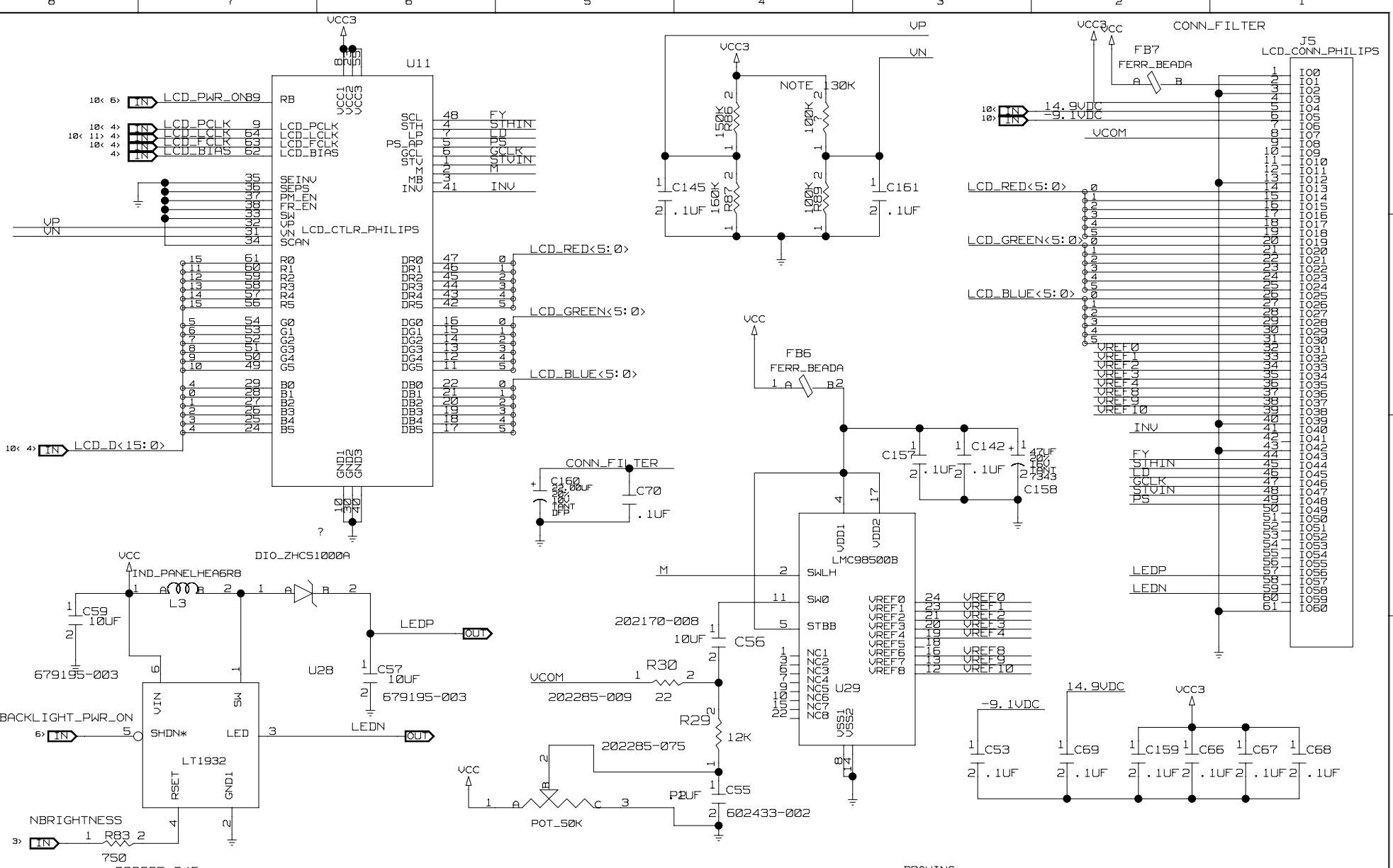
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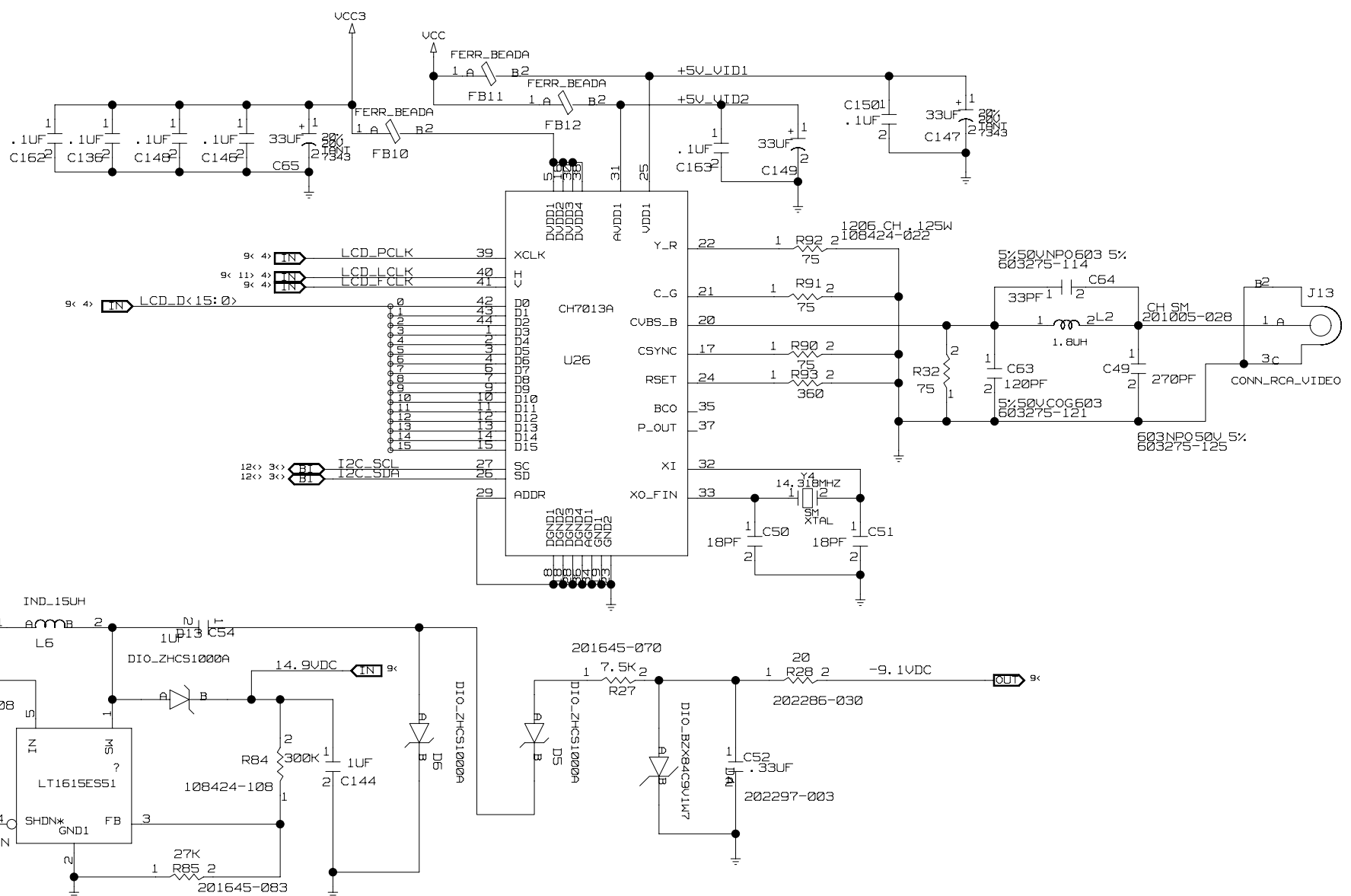
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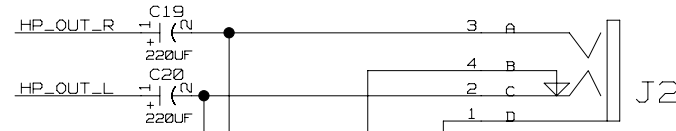
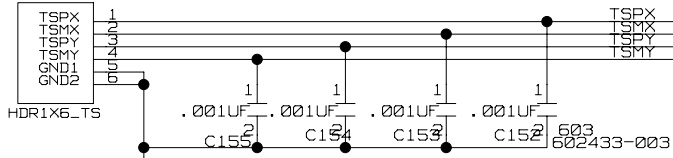
[PAGE_TITLE= NTSC ENCODER AND LCD POWER]

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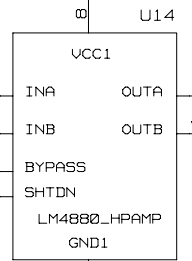
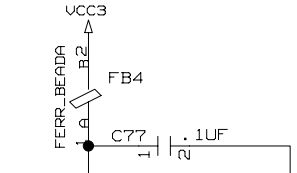
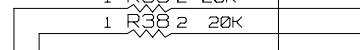
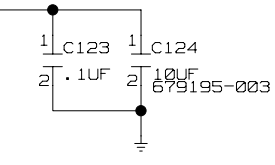
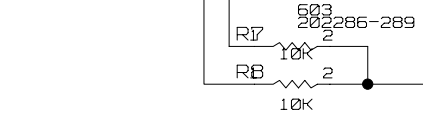
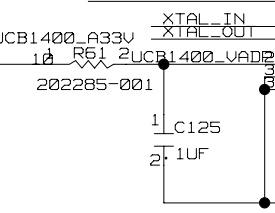
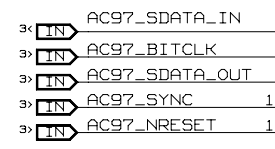
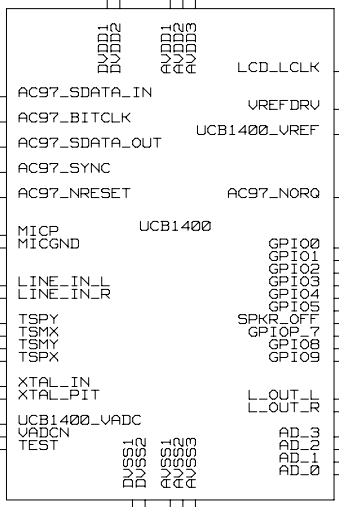
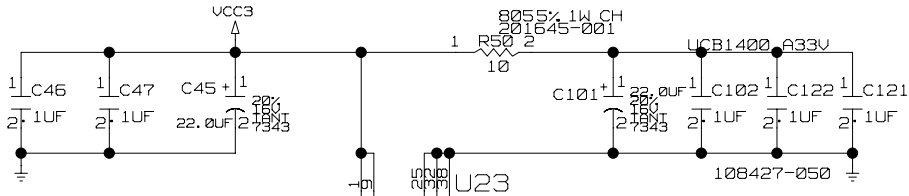
TOUCH SCREEN CONNECTOR

J6



SPEAKER CONNECTOR

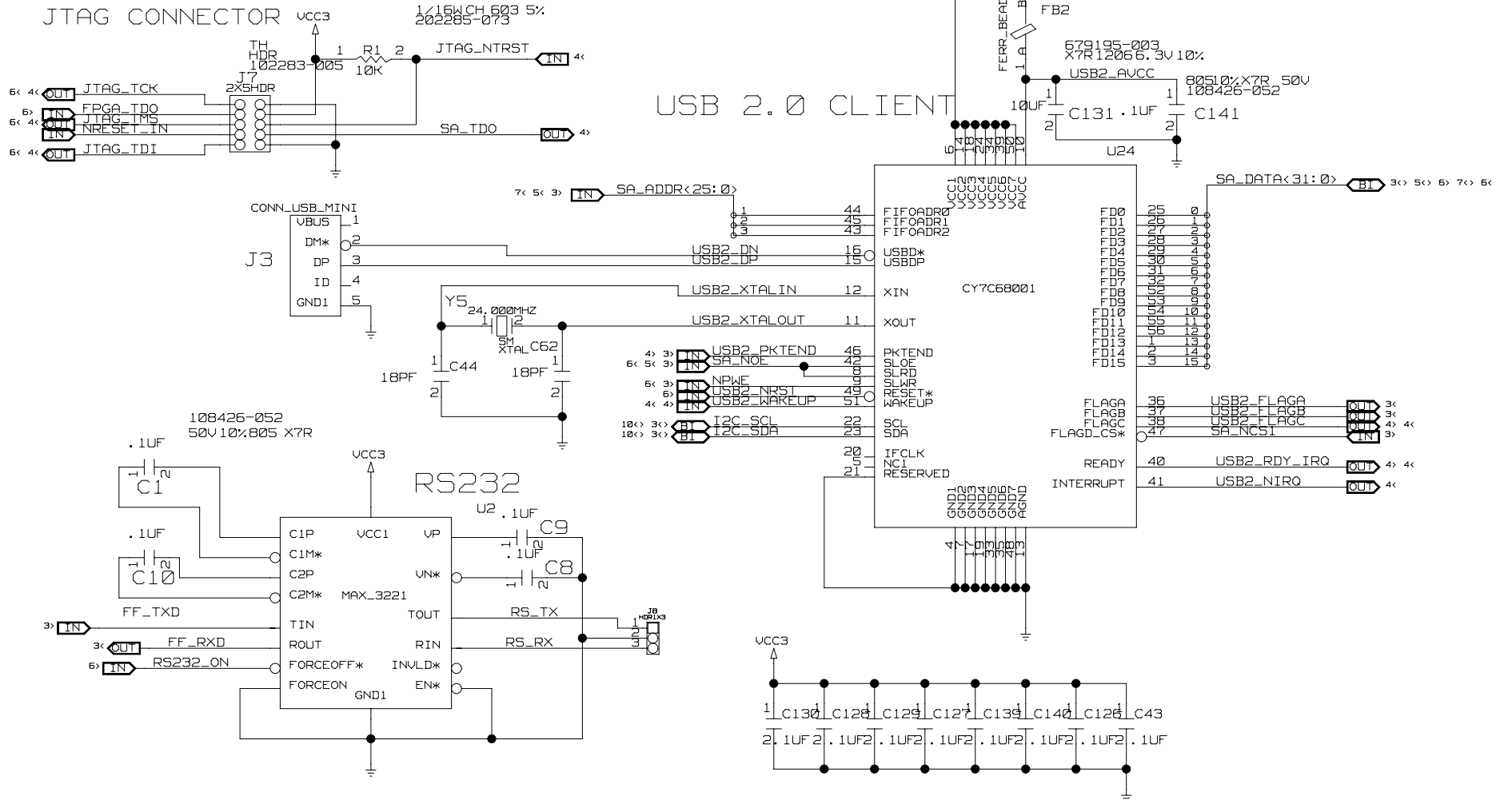
J20



DRAWING PMP_SCH-1.11 Tue Jul 27 14:28:04 2004

[PAGE_TITLE= UCB1400 AUDIO, TOUCH SCREEN]

INTEL	DOCUMENT NUMBER	PAGE	REV
	CXXXXX	11	

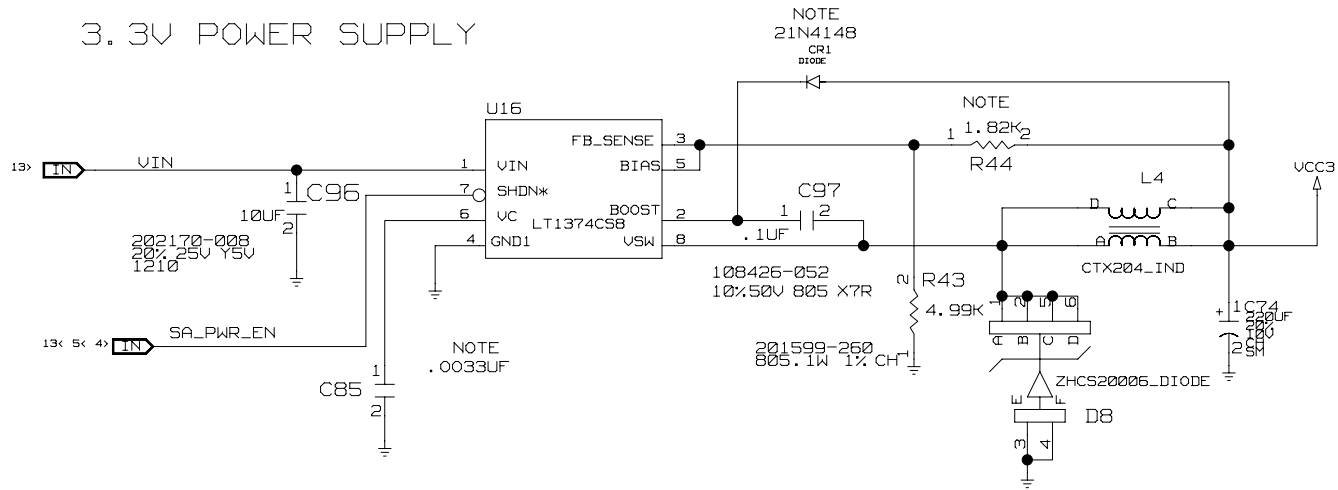


[PAGE_TITLE= USB 2.0 RS232 AND JTAG]

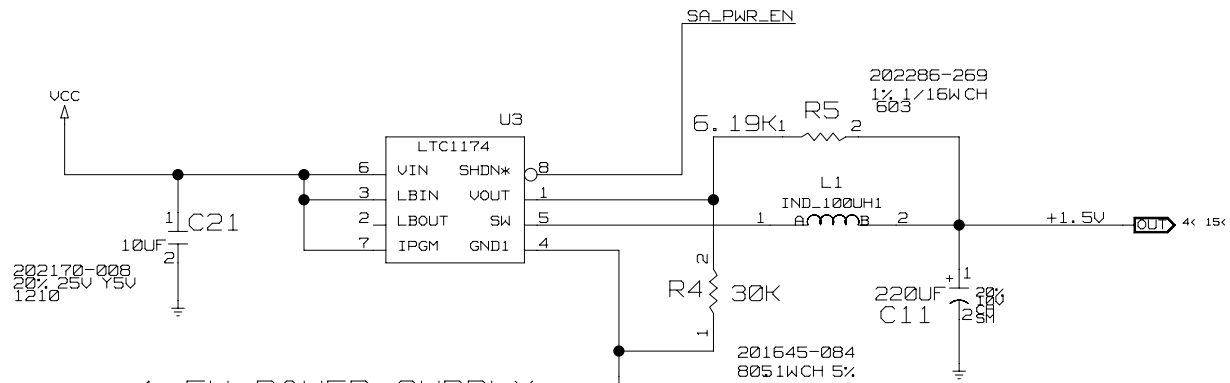
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Fri Dec 19 16:20:33 2003

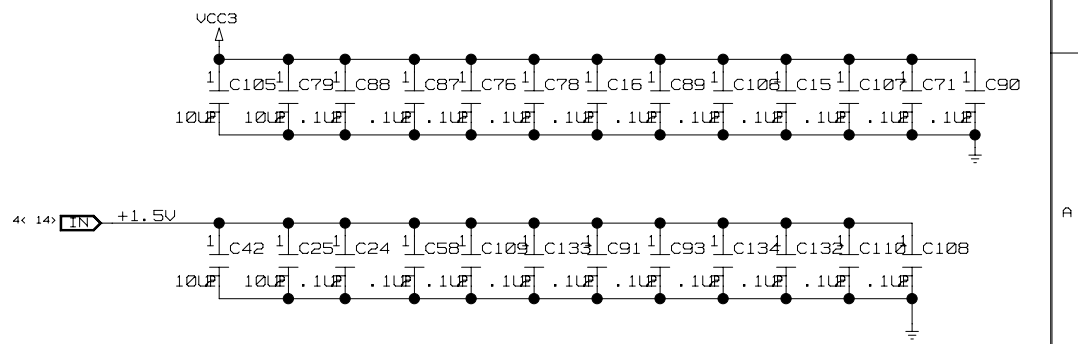
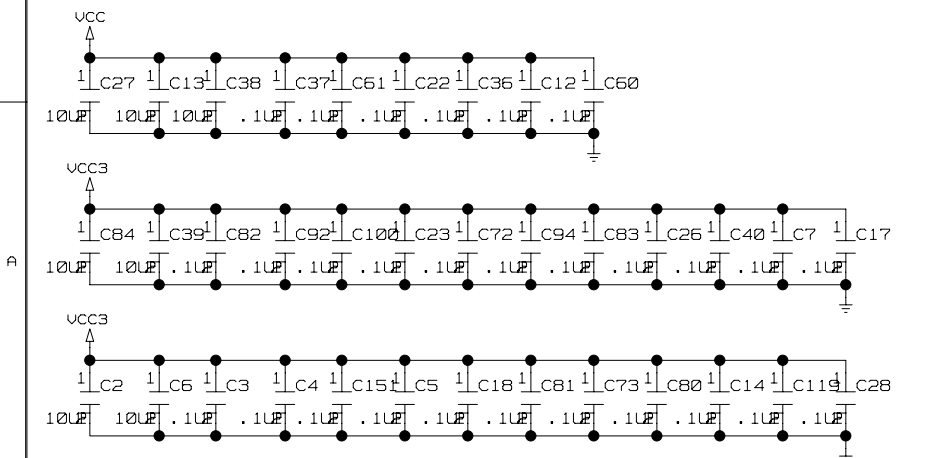
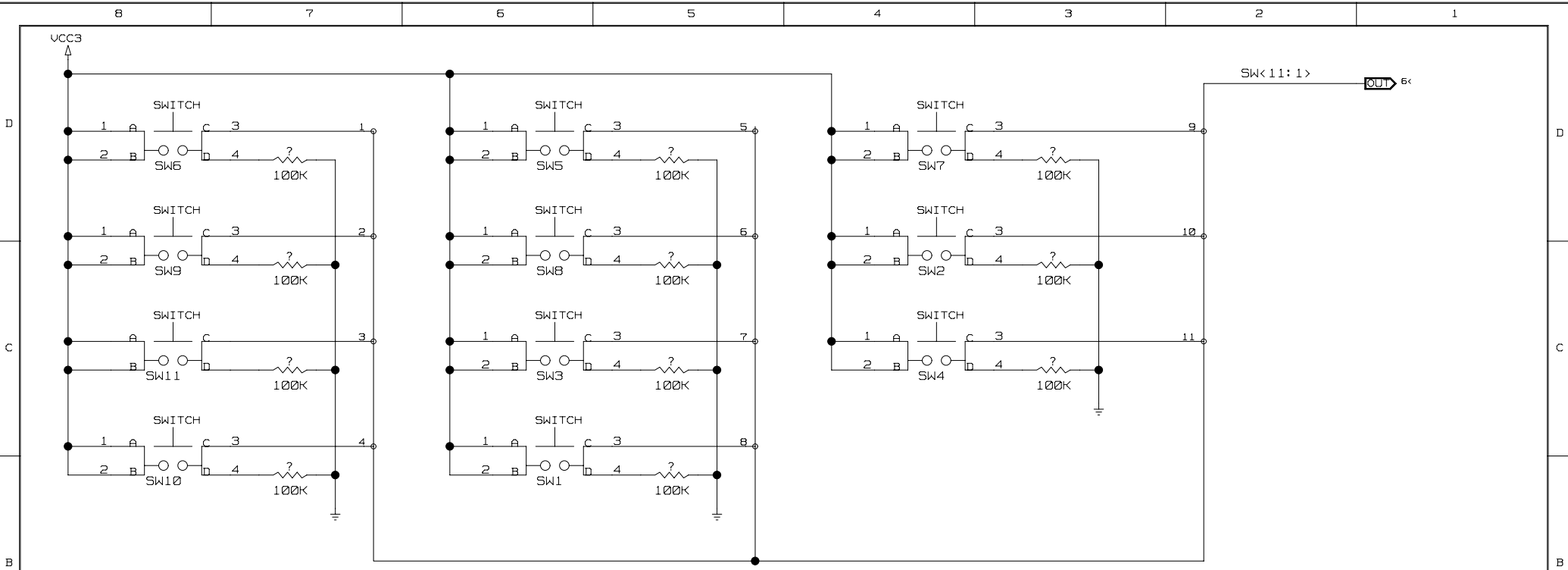
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	C31974	12	

3.3V POWER SUPPLY



1.5V POWER SUPPLY

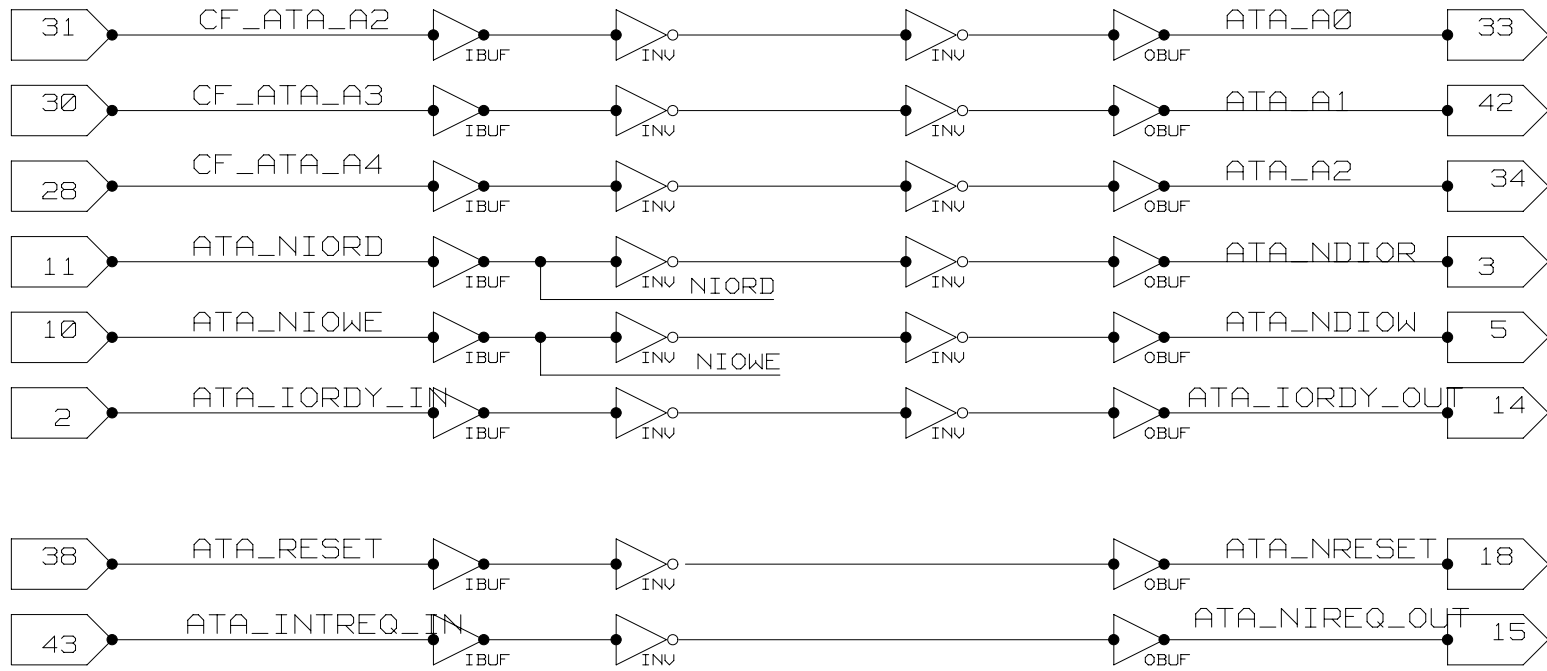




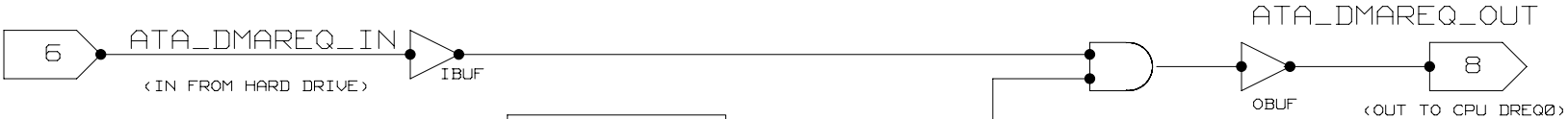
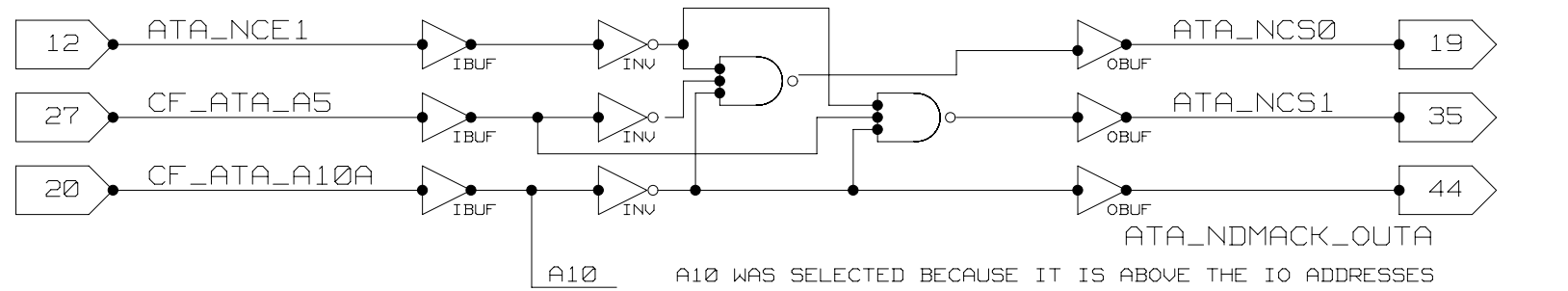
[PAGE_TITLE= BUTTONS AND BYPASS]

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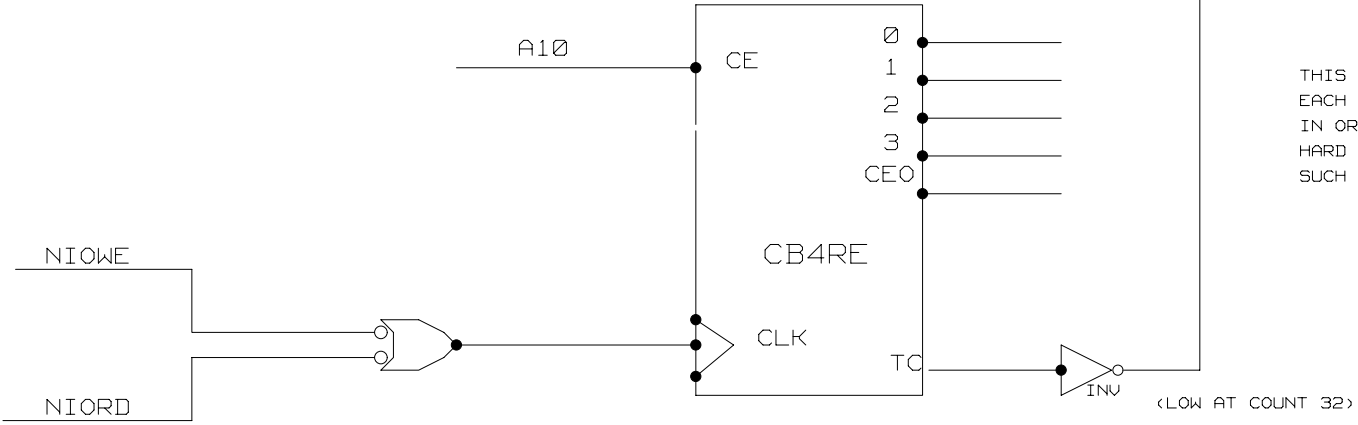
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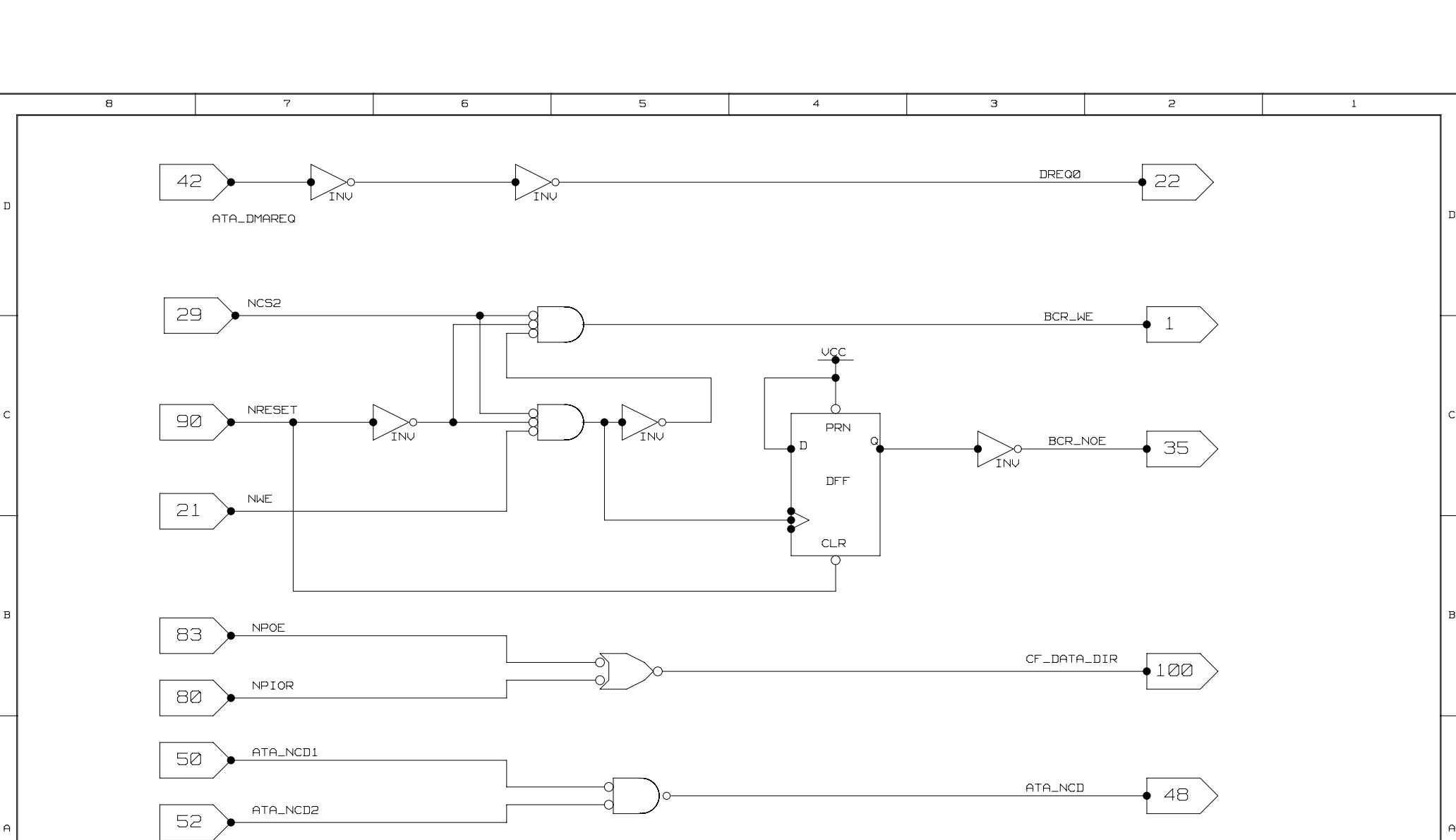
XILINX* CPLD PAGE 1



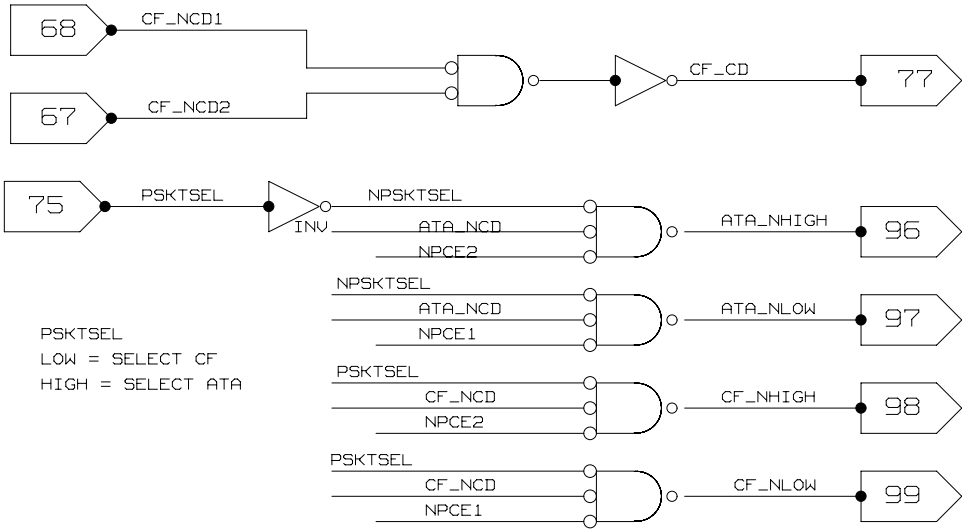
THIS TOGGLES DREQ0 AFTER EACH 32 BYTE WRITE OR READ IN ORDER TO SUPPORT HARD DIVE ACCESSES LARGE THAN 32 BYTES SUCH AS A 512 BYTE SECTOR ACCESS



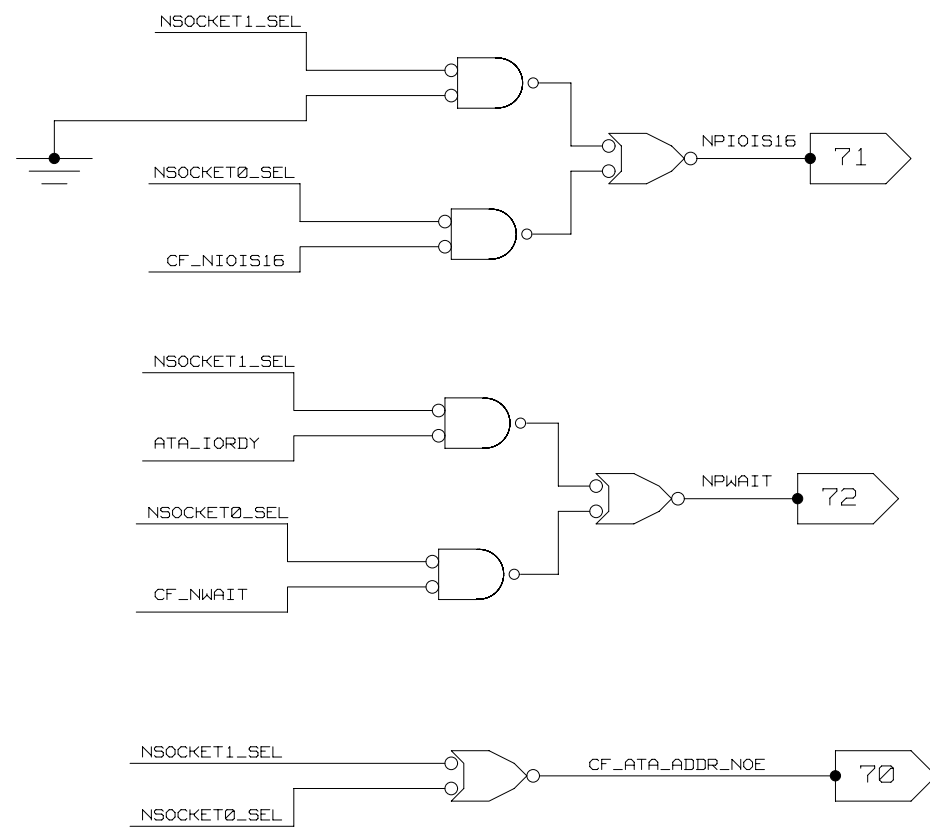
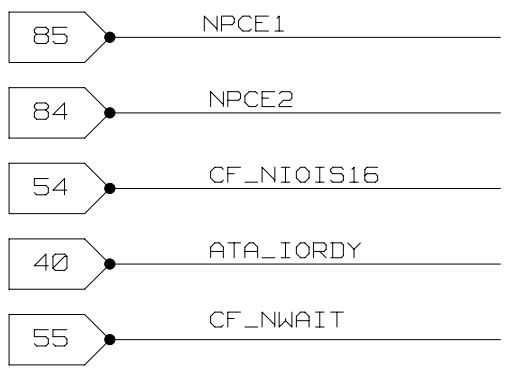
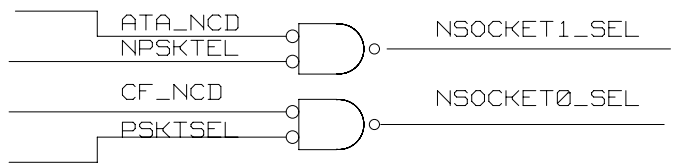
XILINX* CPLD PAGE 2



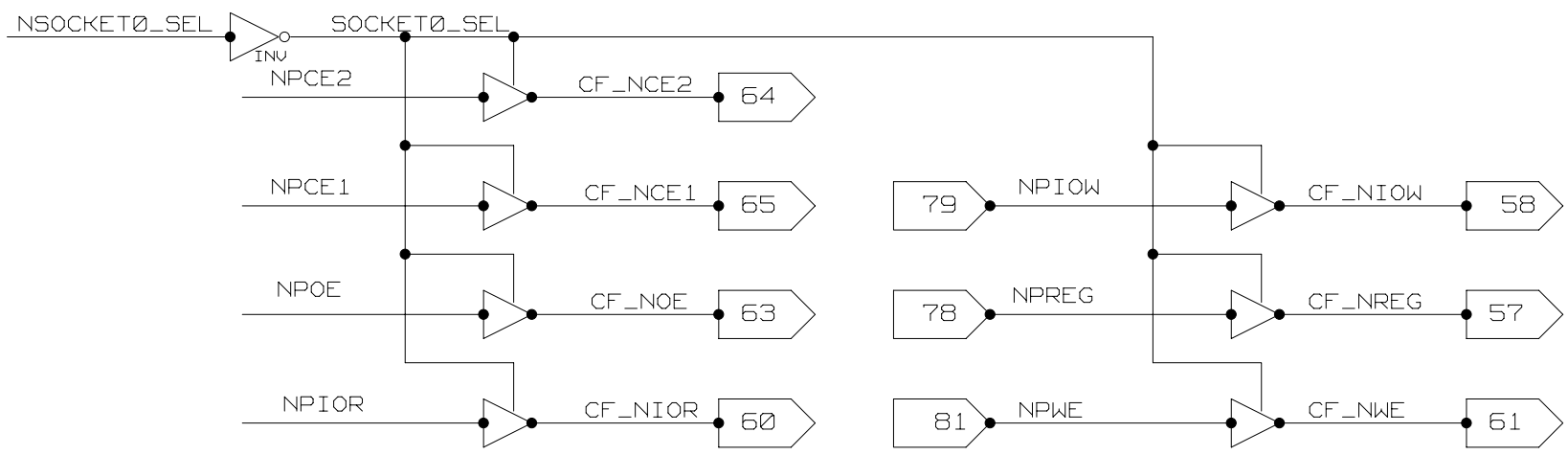
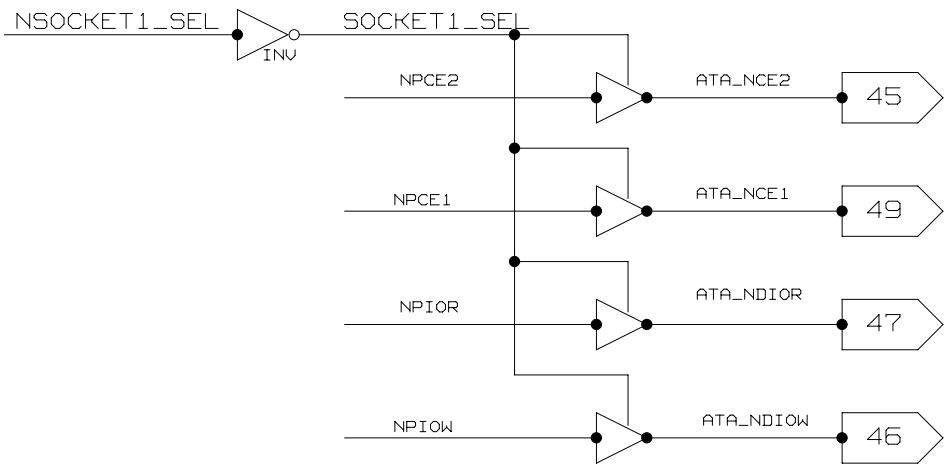
ALTERA* CPLD PAGE 1



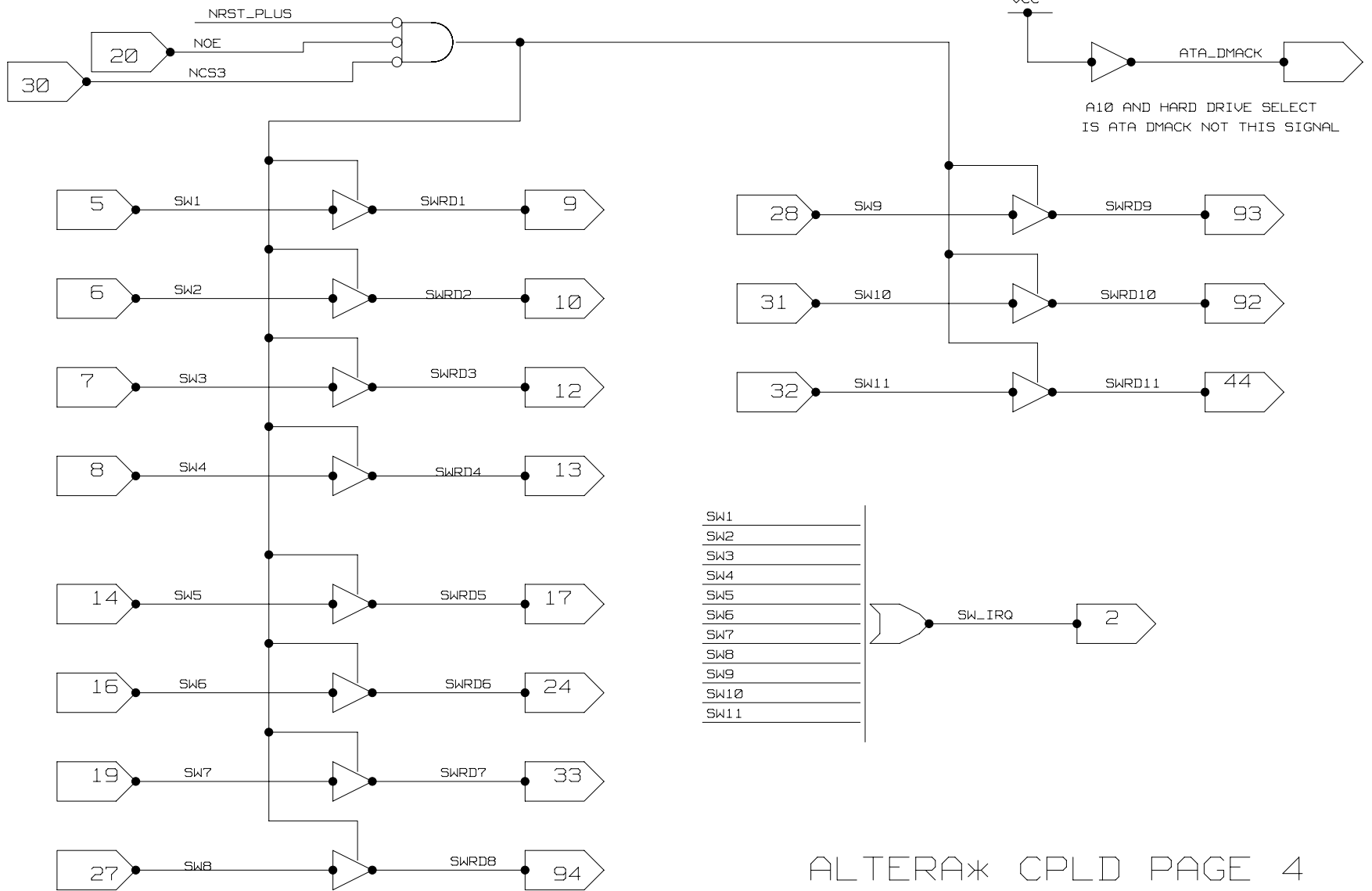
PSKTSEL
LOW = SELECT CF
HIGH = SELECT ATA



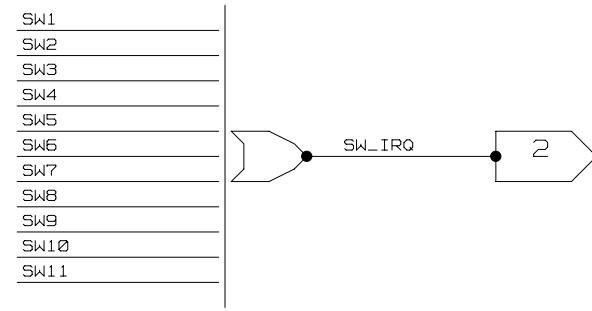
ALTERA* CPLD PAGE 2



ALTERA* CPLD PAGE 3



VCC
 ATA_DMACK
 A10 AND HARD DRIVE SELECT
 IS ATA DMACK NOT THIS SIGNAL



ALTERA* CPLD PAGE 4