Programming CPLD and FPGA Code on the Intel® PXA27x Processor Developer's Kit

Application Note

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Contents

1.0 Introduction 5
1.1 Required Software 5
1.2 Code Updates 5
2.0 Installing a CPLD Transfer Program 5
3.0 Setting Up the Cable Connections 5
3.1 Main Board and Daughter Card Cable Interface for CPLD and FPGA Programming 6
3.2 PMIC (LDO) Card Cable Interface for CPLD Programming 7
3.2.1 Revision 1.2 PMIC (LDO) Cards 8
3.2.2 Revision 1.1 and older PMIC (LDO) Cards 8
4.0 Setting the Switches 9
5.0 Installing the FPGA Code 10
5.1 Using the iMPACT* Application for the Main Board FPGA 10
6.0 Installing the CPLD Code 11
6.1 Using the iMPACT* Application for the Main Board 11
6.2 Using the iMPACT* Application for the Daughter Card or PMIC Card CPLD 11

Revision History

Date	Revision	Description
April 2004	001	Initial version of this document

1.0 Introduction

This application note describes how to program the Complex Programmable Logic Device (CPLD) code and Field Programmable Gate Array (FPGA) code on the Intel® PXA27x Processor Developer's Kit Main Board (main board), the Intel® PXA27x Processor Developer's Kit Daughter Card (daughter card), and the Intel® PXA27x Processor Developer's Kit PMIC (LDO) Card (PMIC card). Follow the steps outlined in this document whenever you need to upgrade the CPLD code or FPGA code on those cards.

1.1 Required Software

To install CPLD or FPGA code onto your system, you need:

- New CPLD or FPGA code file
- CPLD file transfer program, such as iMPACT* from Xilinx

1.2 Code Updates

Each Intel® PXA27x Processor Developer's Kit board or card has its own unique code.

Refer to the *Intel® PXA27x Processor Developer's Kit Main Board Specification Update*, *Intel® PXA27x Processor Developer's Kit Daughter Card Specification Update*, or *Intel® PXA27x Processor Developer's Kit PMIC (LDO) Card Specification Update* for the errata and latest versions of the CPLD or FPGA code needed for your board or card.

2.0 Installing a CPLD Transfer Program

Before you can install new CPLD or FPGA code onto the board or card, you need to install a CPLD file transfer program, such as iMPACT* from Xilinx, on your system.

To download and install the iMPACT* files, go to: http://www.xilinx.com/

You can use other CPLD transfer programs, however, the following instructions are specific to the iMPACT* program.

3.0 Setting Up the Cable Connections

You need to connect to your board or card in order to load the code. The instructions for connecting the main board or the daughter card are the same. However, the PMIC card has its own connection instructions.

3.1 Main Board and Daughter Card Cable Interface for CPLD and FPGA Programming

To connect to the main board or daughter card, connect the Intel® JTAG cable to the J4 connector on the daughter card.

Figure 1. Connectors, Intel® PXA27x Processor Developer's Kit Daughter Card (Revision 1.0)

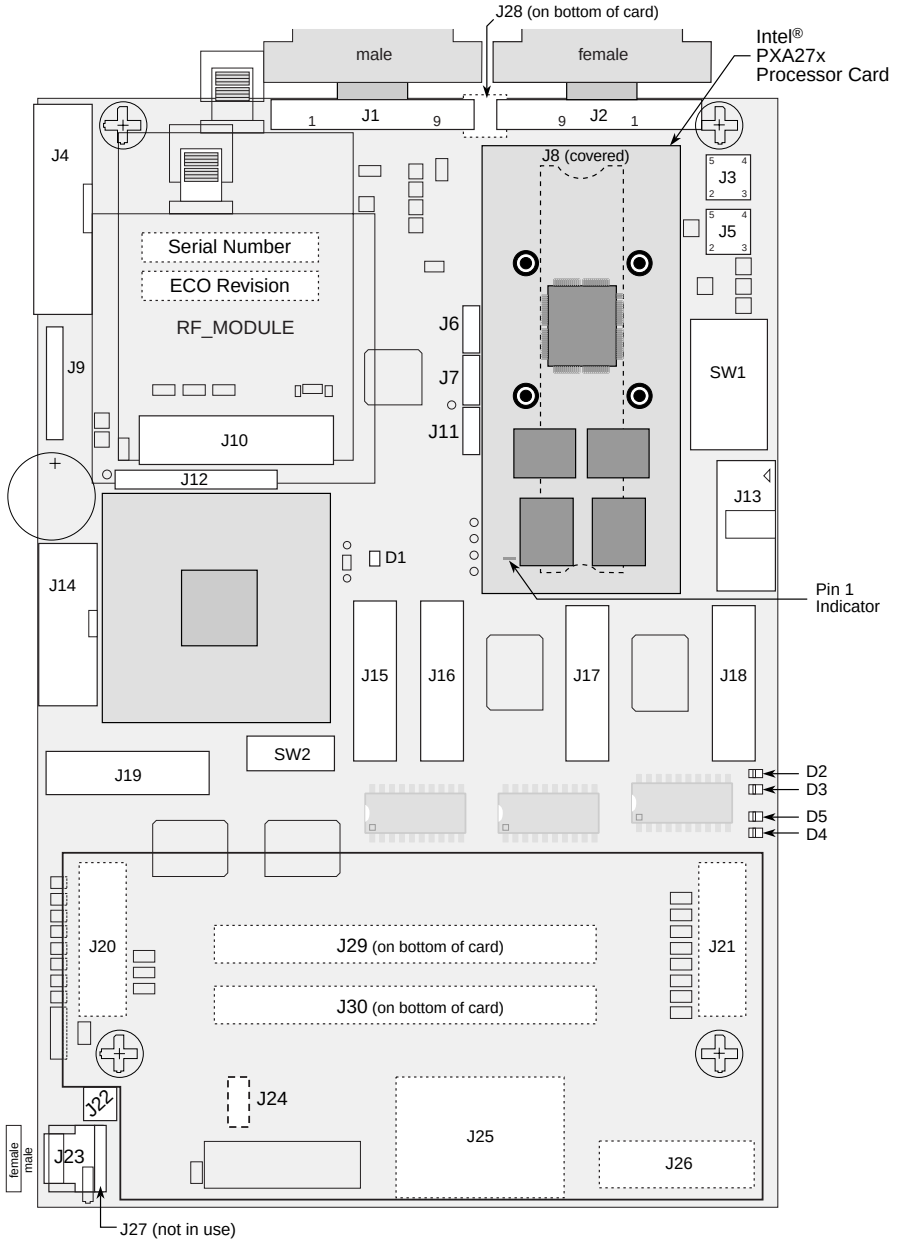
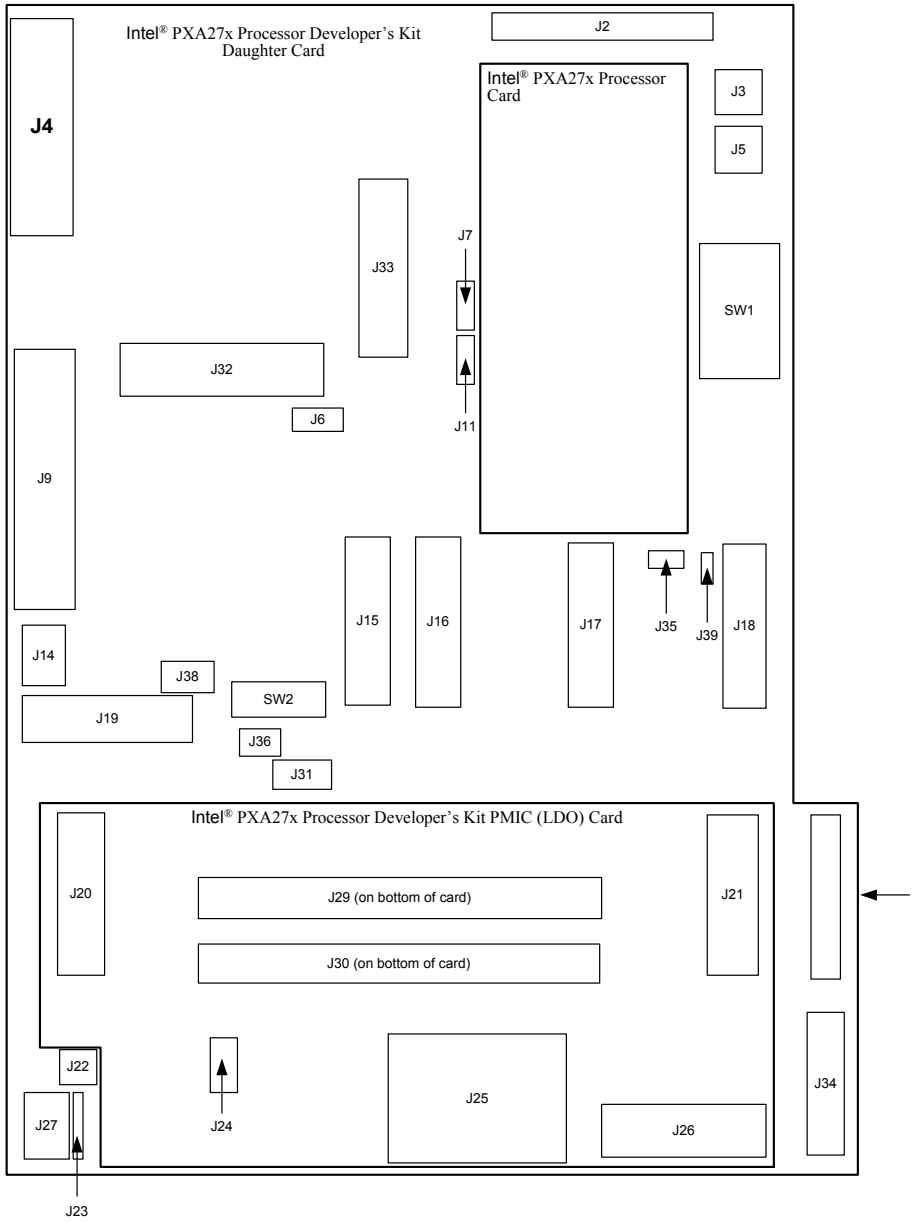


Figure 2. Connectors, Intel® PXA27x Processor Developer's Kit Daughter Card (Revision 1.2)



3.2 PMIC (LDO) Card Cable Interface for CPLD Programming

The version of the PMIC card that you are using, determines the set of instructions that you need to follow to set up the cable interface.

3.2.1 Revision 1.2 PMIC (LDO) Cards

For revision 1.2 PMIC cards, configure the cable interface the same way that you would for the main board or daughter card as listed in section, "Main Board and Daughter Card Cable Interface for CPLD and FPGA Programming".

3.2.2 Revision 1.1 and older PMIC (LDO) Cards

To connect to the PMIC card, use an Insight* connector model IJC-1 or IJC-2 cable. Configure the cable as follows:

- P1= Vcc (Red)
- P2= Gnd (Gnd, black)
- P3= Tck (White)
- P4= TD0 (White)
- P5= TDI (White)
- P6= TMS (White)

For programming the CPLD code on the PMIC card, use the JP1 cable interface. You do not need to make any switch configurations for the PMIC card.

PMIC card cable extension from the Intel® JTAG cable:

LDO J1 Intel® JTAG Cable J1

6 ---------- TMS ---------- 7

5 ---------- TDI ---------- 5

4 ---------- TDO ---------- 13

3 ---------- TCK ---------- 9

2 ---------- GND ---------- 20

1 ---------- 3.3V ---------- 1

Note: Pins 1 and 2 on the Intel® JTAG cable must be connected to 3.3 volts. You can either open the Intel® JTAG cable enclosure and solder a short between pins 1 and 2, or pigtail the cable as shown above.

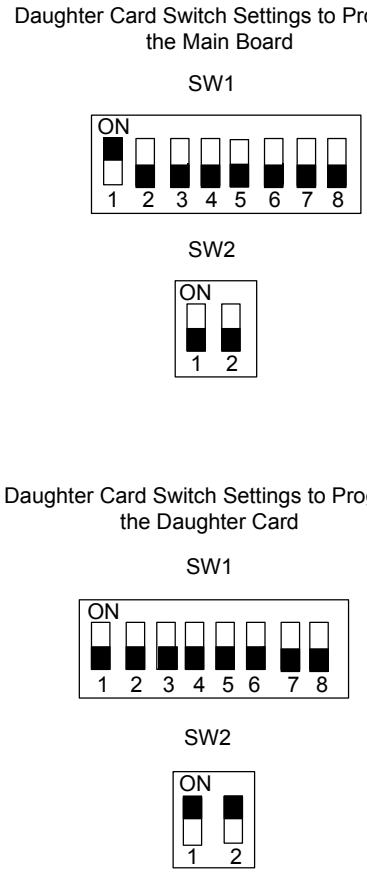
Pin layout of Intel® JTAG cable J1 - Connected to short flat ribbon cable

```
+--------------------------------------+
|    2 4 6 8 10 12 14 16 18 20       |
|    1 3 5 7 9 11 13 15 17 19        |
| (viewed from Bottom of Intel® JTAG cable)|
+--------------------------------------+
```

4.0 Setting the Switches

To update code on the main board or daughter card, you need to adjust the SW1 and SW2 switches. The following illustration shows the switch positions for upgrading the code.

Figure 3. Switch Settings for Downloading CPLD and FPGA Code



For upgrading code on the main board, SW1(1) must be in the up position and SW2 (1,2) must be in the down position. For upgrading code on the daughter card, SW1(1) must be in the down position and SW2 (1,2) must be in the up position. SW2(2,3,4,5,6,7,8) do not influence code programming.

Note: You do not need to configure any switch settings for programming the CPLD or FPGA code on the PMIC card.

5.0 Installing the FPGA Code

This section describes how to install the new FPGA code.

5.1 Using the iMPACT* Application for the Main Board FPGA

Follow these steps to install the new FPGA code on the main board.

1. Open the iMPACT* application.
2. Select “Configure Devices”, then click “Next”.
3. Select “Boundary Scan mode”, then click “Next”.
4. Select “Automatically connect to cable and identify Boundary -Scan chain”.
5. Next, click “Finish”. The system initially executes and opens a program window “untitled (configuration Mode) - iMPACT.” The application then generates three device icons.
6. Double click on the third device icon, skipping the first two.
7. Select the two currently supported files.
8. To assign a “New Configuration File”, choose the file ms2_mainbrd_fpga_1_03.mcs and then click “Open”.
9. For the “Device Select Part Name”, choose xc18v and click OK.
10. Right click on the right-most device icon and choose “Program” from the pop-up window.
11. For program options, select:
    - erase before programming
    - verify
    - use D4 for CF
12. Then click “OK”.
13. Wait for a message indicating that the program succeeded. Then close the window and power cycle the machine.

6.0 Installing the CPLD Code

6.1 Using the iMPACT* Application for the Main Board

1. Open the iMPACT* application.
2. Select “Configure Devices”, then click “Next”.
3. Select “Boundary Scan mode”, then click “Next”.
4. Select “Automatically connect to cable and identify Boundary -Scan chain”.
5. Next click “Finish”. The system initially executes and opens a program window “untitled (configuration Mode) - iMPACT.” The system then displays three device icons.
6. Double click on the first device icon, select the currently supported “JED file”.
7. Move the mouse into the icon, right click on it, and select Program. The Program options window will pop up. Check the following two options:
   — “Erase Before programming”
   — “Verify” (OK)

iMPACT* starts “executing command” and programs the CPLD code.

6.2 Using the iMPACT* Application for the Daughter Card or PMIC Card CPLD

1. Open the iMPACT* application.
2. Select “Configure Devices”, then click “Next”.
3. Select “Boundary Scan mode”, then click “Next”.
4. Select “Automatically connect to cable and identify Boundary -Scan chain”.
5. Next click “Finish”. The system initially executes and opens a program window “untitled (configuration Mode) - iMPACT.” The system then displays one device icon.
6. Double click on the device icon, select the currently supported “JED file”.
7. Move the mouse into the icon, right click on it, and select Program. The Program options window will pop up. Check the following two options:
   — “Erase Before programming”
   — “Verify” (OK)

iMPACT* starts “executing command” and programs the CPLD code.