



# ***Connecting NAND Flash to the Intel® PXA27x Processor Family***

**Application Note**

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***October 2004***



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## 1.0 Introduction

NAND Flash has performance characteristics, pricing, and memory size options that make it appealing for use in some PXA27x Processor Family designs. PXA27x processors natively support NOR Flash. NAND Flash is significantly different from NOR Flash and is not natively supported by PXA27x processors. There are, however, software and hardware methods for connecting PXA27x processors to some types of NAND Flash.

This application note provides a basic understanding of the considerations involved with connecting a NAND Flash chip to a PXA27x family processor. General characteristics, behaviors, and signal names of NOR and NAND Flash are discussed. Carefully review the datasheets, application notes, and guides for any specific NAND chip being considered. The NAND Flash discussed in this application note supports an operation mode called “CE don’t care” during read, program, and the  $t_R$  “busy” period.

## 2.0 NAND Overview

### 2.1 NAND Signals

NOR Flash is connected via address and data pins similar to other memory devices. NAND Flash uses a multiplexed I/O interface and additional control signals. A typical NAND device has the following signals:

- I/O 0-7 (or I/O 0-15) - address and data bidirectional IO signals
- $\overline{CE}$  - Chip Enable
- AL - Address Latch Enable
- CL - Command Latch Enable
- $\overline{RE}$  - Read Enable
- $\overline{WE}$  - Write Enable
- R/B - Ready/Busy
- $\overline{WP}$  - Write Protect

These signals must be mapped to PXA27x signals to read and write to NAND.

### 2.2 NAND Structure

NOR Flash is divided into blocks. Each block contains many words that are typically 16 bits wide. Frequently in PXA27x designs, two 16-bit NOR chips are used in parallel to provide a 32-bit width. NOR Flash allows random access to stored data words. The read operation is a simple operation of placing the desired word address on the address bus and then reading that data off the data bus. Erases and lock operations are managed at the block level. Individual words can be programmed after a block has been erased.

Like NOR Flash, NAND Flash is also divided into blocks. However, each NAND Flash block contains many pages instead of words. A typical NAND page consists of 512 bytes. To read or write from NAND, a command sequence is issued to select a block and page. After this selection, the entire page can be read or written.

NAND Flash typically contains blocks that contain errors and cannot be used. Software accessing NAND must establish and maintain a table of bad blocks. Software must also use techniques such as checksums and error-correcting systems to ensure data integrity.

## 3.0 Connecting the Intel® PXA27x Processor to NAND

### 3.1 What Type of NAND to Connect to an Intel® PXA27x Processor

A subset of NAND Flash supports a mode called “ $\overline{\text{CE}}$  don't care” operation. During the read and program operations, many NAND chips require the  $\overline{\text{CE}}$  signal to remain steady state throughout operations. NAND Flash that supports “ $\overline{\text{CE}}$  don't care” allows the  $\overline{\text{CE}}$  signal to transition during the NAND access, thus allowing this flash to be connected to active memory buses such as the PXA27x memory bus.

An important aspect of the “ $\overline{\text{CE}}$  don't care” operation occurs immediately after the processor programs an address into the NAND flash. Some NAND flash chip support “ $\overline{\text{CE}}$  don't care” operation but still require  $\overline{\text{CE}}$  to remain low while the  $\text{R}/\overline{\text{B}}$  signal is busy immediately following an address input. This busy period is often referred to as  $t_{\text{R}}$  on NAND datasheets. To avoid compatibility issues ensure that your NAND flash chip treats the  $\overline{\text{CE}}$  signal as a “don't care” during normal read operations as well as the  $t_{\text{R}}$  period. There are several NAND chips on the market that support this type of operation.

### 3.2 Signal Mapping

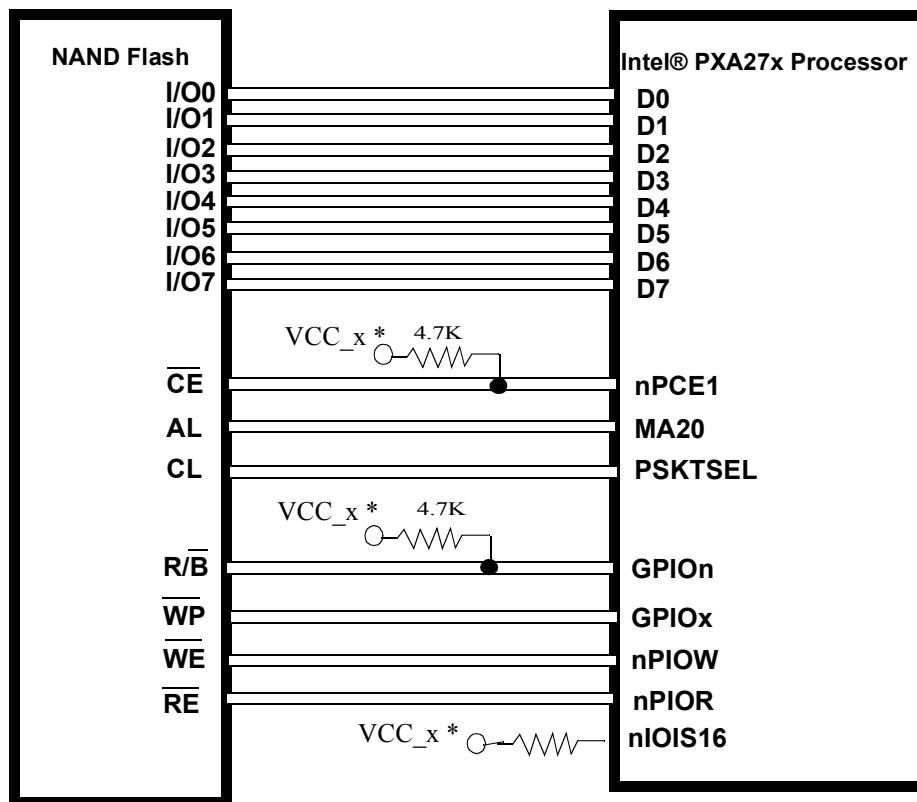
The PXA27x processor PCMCIA interface can be approximately mapped to NAND signals. The PCMCIA interface was selected because of the many available timing options and because using dedicated PCMCIA memory signals such as  $\text{pCE1}$ ,  $\text{nPIOR}$ , and  $\text{PKTSEL}$  minimize the amount of extra signal transitions the NAND Flash sees while other memory-bus operations are occurring. System designers can choose different signals and connections from the ones described here; however, designers should be aware that different types of NAND can be sensitive to being connected to an active memory bus. In worst cases, more buffer logic may be needed to shield a NAND chip from extraneous memory-bus signal transitions.

- Connect the NAND IO pins to the PXA27x memory-controller data pins, D0 to D7 or D0 to D15. This connections lets the processor write the preferred command and address values to the IO pins, and reads back the results over these same pins.
- Connect the NAND  $\overline{\text{CE}}$  signal to the PXA27x PCMCIA  $\text{nPCE1}$  signal. To prevent erroneous  $\text{nPCE1}$  assertion during system reset, ensure this signal has a 4.7K pull-up.
- Connect the NAND AL signal to a PXA27x address pin. This connection allows the AL signal to be a 1 or 0, depending on the PCMCIA address being accessed. For example, connecting the NAND AL signal to PXA27x MA20; accesses to PCMCIA IO address 0x0010\_0000 would be decoded as a NAND address (AL=1) operation.

- Connect the NAND CL signal to the PXA27x PCMCIA PSKTSEL signal to allow software to perform NAND command operations (CL=1) by accessing the PCMCIA address space for PCMCIA Card 1. All other software NAND operations (CL=0) are performed by accessing the PCMCIA address space for PCMCIA Card 0.
- Connect the NAND R/B signal to a PXA27x GPIO pin. This signal usually is an open drain signal and needs a pull-up resistor on most types of NAND Flash.
- Connect the NAND WP signal to a PXA27x GPIO for software-controlled write protection. Alternately, this signal can be tied high to disable write protection entirely.
- Connect the NAND WE signal to the PXA27x nPIOW signal.
- Connect the NAND RE signal to the PXA27x nPIOR signal.
- To connect 16-bit wide NAND chips, tie the PXA27x PCMCIA signal nIOIS16 low to ensure PCMCIA IO transactions are treated as 16-bit transactions. For 8-bit wide NAND chips, tie the nIOIS16 signal high to make the PCMCIA memory controller perform 8-bit operations only.

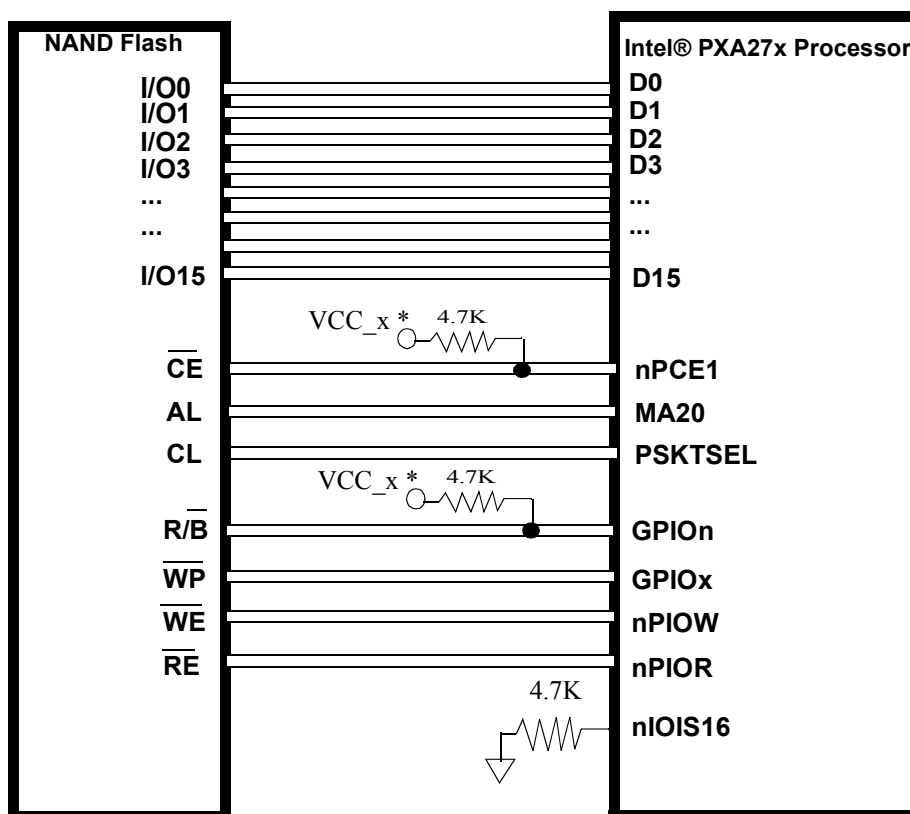
## 4.0 Connection Diagrams

### 4.1 8-Bit NAND to the Intel® PXA27x Processor



**NOTE:** \*VCC\_x: Ensure the pull-ups used for nIOIS16, CE and R/B are pulled up to the correct PXA27x voltage domain as specified in the PXA27x EMTS Pin Usage Summary. These voltage domains should match the VCC\_MEM voltage so that all logic levels going into the NAND chip are the same.

## 4.2 16-Bit NAND to the Intel® PXA27x Processor



**NOTE:** \*VCC\_x: Ensure the pull-ups used for  $\overline{CE}$  and  $R/\overline{B}$  are pulled up to the correct PXA27x voltage domain as specified in the PXA27x EMTS Pin Usage Summary. These voltage domains should match the VCC\_MEM voltage so that all logic levels going into the NAND chip are the same.

## 5.0 Intel® PXA27x Configuration

### 5.1 Intel® PXA27x GPIO Alternate Function Choices and GPIO Directions

Several of the PCMCIA signals used to connect PXA27x processor to NAND are GPIO pins that must be configured as alternate functions. Depending on the function of the GPIO, they also must be configured as an input or output. Some alternate functions are available on more than one GPIO so system designers have flexibility in which GPIO pins are used. See the *Intel® PXA27x Processor Family Developers Manual* for detailed descriptions of the registers and instructions for configuring GPIO directions and alternate functions.

The GPIOs with alternate functions used in this application note are as follows:

- GPIO 15, GPIO 85, GPIO 86 or GPIO 102 configured as an output and as nPCE<1>
- GPIO 79 or GPIO 104 configured as an output and as PSKTSEL

- GPIO 50 configured as an output and as PIOR
- GPIO 51 configured as an output and as PIOW
- GPIO 57 configured as an input and as nIOIS16

Use any available GPIO as an output to connect to the NAND  $\overline{WP}$  signal. Similarly, any available GPIO can be used as an input for the NAND ready/busy signal.

Ensure that the signals used to connect to the NAND Flash are all operating on the same voltage and logic levels. Information about which power domains power GPIOs is found in the *Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification*. For example, GPIO 50 is used as nPIOR and connected to NAND  $\overline{RE}$ . This signal is powered by VCC\_BB according to the *Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification*. Therefore, ensure VCC\_BB operates at the same voltage as VCC\_MEM to ensure the nPIOR logic levels match the memory-bus logic levels.

## 5.2 Other Intel® PXA27x Register Configuration Settings

There are several other registers in the PXA27x processor that must be configured. These registers are all documented in the *Intel® PXA27x Processor Family Developers Manual*.

Set both the Expansion Memory Configuration register MECR[CIT] and MECR[NOS] to 1 to indicate that the nIOIS16 signal should be considered when accessing PCMCIA addresses and to indicate the PKTSEL signal is also being used.

Set the Power Manager General Configuration register PCFR[FP] bit to a 0 to indicate that the PCMCIA nPCE1, nPIOR, and nPIOW signals should not be floated in sleep mode. Software should program the PGSRx bits correctly so that during sleep mode, the GPIO pins connected to the NAND Flash are in a known good state. It is most important that the nPCE1 signal is held high during sleep mode so that the NAND Flash chip is not active.

The PCMCIA memory timings are discussed in the next section. The MCIOx registers must be configured for proper timing operation. Software and OS driver developers: be aware that many timings are based on the memory-clock frequency. Systems that change frequencies dynamically may need to modify memory timings if the memory-clock frequency is changed.

## 6.0 Intel® PXA27x Memory Timings for Interfacing with NAND Flash

This section compares common NAND timing parameters used across multiple NAND Flash vendors to the PXA27x PCMCIA timing parameters. System designers are advised to do their own similar timing analysis for the particular NAND Flash parts they are interested in using.

Several PXA27x PCMCIA registers are described in this section. Read the *Intel® PXA27x Processor Family Developers Manual* for more register details. For a diagram of the PXA27x PCMCIA memory-signal timings, refer to the *Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification* or the *Intel® PXA270 Processor Electrical, Mechanical, and Thermal Specification*.

The most common timing names, names like  $t_{CS}$ , are listed with each of the following sections. Some NAND Flash vendors have different meanings for some of these timings. Carefully review the timings for any specific NAND chip before trying to connect it to a PXA27x processor.

## 6.1 $\overline{CE}$ , CLE, and ALE Setup Times ( $t_{CS}$ , $t_{CLS}$ and $t_{ALS}$ ),

The  $\overline{CE}$  chip-enable signal is the first signal to change when a NAND transaction occurs. A setup time is required before the rising edge of the NAND  $\overline{WE}$  signal. A typical  $\overline{CE}$  setup time is approximately 35ns.

A setup time from the rising edge of the CLE and ALE signals to the rising edge of the NAND  $\overline{WE}$  signal is also required. The CLE and ALE setup time is similar but generally shorter than the  $\overline{CE}$  setup time.

$\overline{CE}$ , CLE, and ALE setup timings are met by the PXA27x PCMCIA memory controller by defining the length of the  $\overline{WE}$  (nPIOW) pulse and adding in extra time with the  $x\_SET$  value of the PXA27x MCIOx registers.

Using a 104 MHz memory clock for the following calculations, a MCIOx[x\_SET] value of 4 would result in the nPCE<x> signal being asserted 19 ns before the nPIOR or nPIOW signals are asserted. A MCIOx[ASST] value of 0 gives nPIOW a length of 5 memory clocks on a write and nPIOR a length of 6 memory clocks on a read. This equals a 48 ns nPIOW length and a 58 ns nPIOR length. Adding these values together gives a total setup time of 77 ns for  $\overline{CE}$ , CLE and ALE before the rising edge of nPIOW ( $\overline{WE}$ ).

## 6.2 $\overline{CE}$ to $\overline{RE}$ Timing Requirements

Some NAND requires a delay between the assertion of  $\overline{CE}$  and the assertion of  $\overline{RE}$ . The MCIOx[x\_SET] field sets up a delay before nPIOR ( $\overline{RE}$ ) is asserted. Following the previous paragraph's example: Using a 104 MHz memory clock, a MCIOx[x\_SET] value of 4 would result in the nPCE<x> ( $\overline{CE}$ ) signal being asserted 19 ns before the nPIOR ( $\overline{RE}$ ) signal being asserted.

## 6.3 $\overline{WE}$ and $\overline{RE}$ Pulse Widths ( $t_{WP}$ and $t_{RP}$ )

$\overline{WE}$  and  $\overline{RE}$  pulse widths are typically 25 to 40 ns. The length of the nPIOW and nPIOR are defined by the  $x\_ASST\_WAIT$  and  $x\_ASST\_HOLD$  as determined by the MCIO0/1[ASST] registers. For example, a programmed value of 0 gives nPIOW a length of 5 memory clocks on a write and nPIOR a length of 6 memory clocks on a read. Assuming a memory clock of 104 MHz this equals a 48 ns  $\overline{WE}$  (nPIOW) length and a 58 ns  $\overline{RE}$  (nPIOR) length.

## 6.4 $\overline{CE}$ , ALE, and CLE hold time ( $t_{CH}$ , $t_{ALH}$ , and $t_{CLH}$ )

During a  $\overline{WE}$  write, NAND typically requires a  $\overline{CE}$ , ALE, and CLE hold time. A typical value for these hold times is 10 ns. The PXA27x PCMCIA controller has an  $x\_HOLD$  timing parameter that is configured by the MCIO0/1[HOLD] register bits. This establishes how long the address, PSKTSEK and PCE<x> signals is held. With a memory clock speed of 104 MHz, a value of 4 in this register field holds these signals for 38 ns past the  $\overline{WE}$  (nPIOW) signal's rising edge.

## 6.5 Data Setup Time ( $t_{DS}$ )

During a write operation, NAND Flash requires the data be established on the NAND IO pins before the rising edge of the  $\overline{WE}$  (nPIOW) signal. A typical value for the data setup is 20 ns. The PXA27x PCMCIA memory controller puts the data on the data bus  $tedDVCL$  (typical = 1 mem clock) before the falling edge of the nPIOW signal and continues to hold the data until after the rising edge of nPIOW. The data is therefore valid on the IO pins for the entire  $\overline{WE}$  (nPIOW) pulse, which easily meets any setup time requirements.

## 6.6 Data Hold Time ( $t_{DH}$ )

During a write operation, NAND Flash requires data to be held on the NAND IO pins for a period of time after the rising edge of the  $\overline{WE}$  signal. A typical NAND Flash data hold time is approximately 10 ns. The PXA27x value of  $tedCHWDI$  specifies how long the data remains on the memory bus after  $\overline{WE}$  (nPIOW) goes high. According to the *Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification*, the typical value is 4 memory clocks. Therefore, at a memory-clock speed of 104 MHz, the hold timing for data would be approximately 38 ns.

## 6.7 WE High Hold Time and Write Cycle Time ( $t_{WH}$ and $t_{WC}$ )

NAND flash requires a delay between consecutive write operations. A typical  $\overline{WE}$  high requirement is 15 ns. A typical minimum total write cycle time of 45 ns. The PXA27x processor can meet these timing requirements with the  $MCI0x[hold]$  timing values. A value of 4 in the  $MCI0x[hold]$  register field at a memory-clock speed of 104 MHz holds the  $\overline{WE}$  (nPIOW) signal high for 38 ns after the signal's rising edge.

## 7.0 NAND Software Considerations

Software must use special procedures to read and write NAND Flash when it is connected as described in this application note. Reads and writes must occur at specific PCMCIA addresses to obtain the appropriate PCMCIA and memory signals to transition.

Be sure to use the correct-sized accesses when reading and writing to NAND. For example, if the NAND width is 16 bits, software should perform only half-word (16-bit) reads and writes to the NAND.

**Note:** All the specific NAND accessing instructions and memory addresses in this section assume the NAND Flash has been connected as described earlier in this application note; NAND AL connected to the PXA27x MA20, and NAND CL connected to the PXA27x PKTSEL. Different

connections can be used to toggle the AL and CL signals; however, the read and write instructions in the following paragraphs would need to be modified for different implementations.

## 7.1 Address Writes to NAND (AL=1, CL=0)

Writing to PXA27x PCMCIA Socket 0 IO addresses with address signal MA20 high are treated as a NAND address operation. The PXA27x PCMCIA Socket 0 IO address space begins at physical address 0x2000\_0000. Therefore, a write to physical address 0x2010\_0000 is decoded as a NAND address write.

## 7.2 Command Writes to NAND (AL=0, CL=1)

Writing to PCMCIA Socket 1 IO addresses with MA20 low is treated as a NAND command operation. The PXA27x PCMCIA Socket 1 IO address space begins at address 0x3000\_0000. Therefore, a write to physical address 0x3000\_0000 is decoded as a NAND command write.

## 7.3 Data Writes to NAND (AL=0, CL=0)

After issuing the command and address information needed to initiate a NAND write, software must perform a series of writes with both CL and AL = 0 by performing writes to the PXA27x PCMCIA Socket 0 IO address region with address signal MA20 low. As mentioned previously, the PXA27x PCMCIA Socket 0 IO address space begins at address 0x2000\_0000. Therefore, a write to physical address 0x2000\_0000 is decoded as a normal NAND write.

## 7.4 Data and Status Reads from NAND (AL=0, CL=0)

To read in data or status from NAND, both the CL and AL signals should be 0. This can be achieved by reading from the PXA27x PCMCIA Socket 0 IO address region with address signal MA20 low. The PXA27x PCMCIA Socket 0 IO address space begins at 0x2000\_0000. Therefore, a read from physical address 0x2000\_0000 is decoded as a NAND read.

## 7.5 Ready/Busy and Write Protection

Software must use a GPIO connected to the R/B signal to be read the status of the Ready/Busy signal. If a GPIO is used to control the write-protect signal of the NAND flash, then software needs to control this signal to turn on or off write protection.

## 7.6 NAND Page Reading and Writing Procedures

Refer to the specific NAND data sheets for the details of reading and writing data pages in NAND Flash. In general, NAND operations are performed by first writing a command to NAND, writing an address to NAND, and then performing one or more reads or writes.

## 7.7 Error Correction and Bad Block Management

Software used to read and store data on NAND generally uses and Error Correction Code (ECC) to ensure data is kept valid. Software must also perform bad-block management. Consult your NAND Flash vendor to investigate what types of ECC, block management, and OS filesystem software is available. Many embedded operating systems now support NAND filesystems to further simplify NAND usage.

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